

FPGA 1K KIWI NANO FPGA BOARD

Compact FPGA. Easy Development. Nano-Class Footprint.

The **FPGA 1K Kiwi Nano** development board is a highly compact, robust evaluation platform engineered specifically for FPGA education, digital logic experimentation, IP core validation, and low-power embedded-control prototyping. Leveraging the advanced Gowin GW1AN-1S (FN32) architecture, the board packs significant computing density into a small form factor while preserving a practical onboard JTAG debugger. The board is perfectly sized to fit standard breadboards and educational kits.

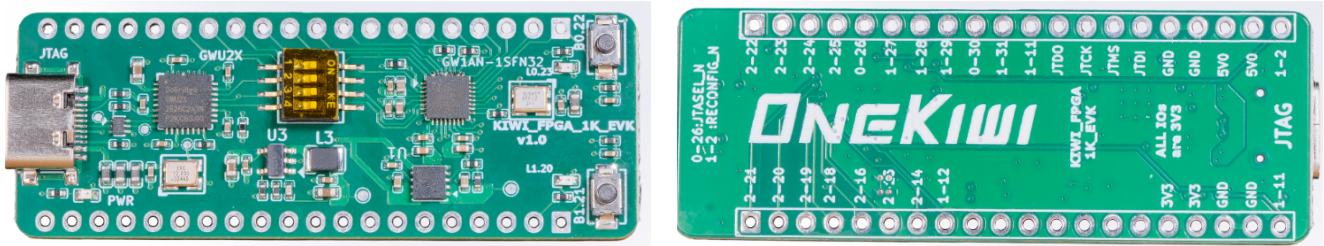


Figure 01. FPGA 1K Kiwi Nano board top-side layout (Left) and Physical Board photo (Right).

Hardware Specifications Table

Parameter	Details	Parameter	Details
FPGA Chip	Gowin LittleBee GW1AN-1S (GW1AN-LV1QN32C6/I5)	Power Main Voltage	5.0 V via USB-C
Logic Resources	1,152 LUT4 Blocks	I/O Operating Voltage	All Header I/Os at 3.3 V
Registers (FF)	864 Flip-Flops (FF)	Embedded Regulators	High-efficiency 3.3V BUCK & 1.2V LDO
Block SRAM	72 Kbit (4 Dedicated BSRAM Blocks)	Physical Dimensions	58.34 mm x 21.29 mm (Nano-class)
User Flash	On-Chip Integrated SPI NOR Flash	Onboard Interface	Dual row headers, 2.54 mm Pitch
Number of PLLs	1 Phase Locked Loop (PLL)	Retail Pack Suite	Board, USB-C Cable, Headers, Retail Box
Onboard Debugger	Integrated USB-JTAG (GWU2X)	Target Use Cases	FPGA Learning, Labs, Prototyping

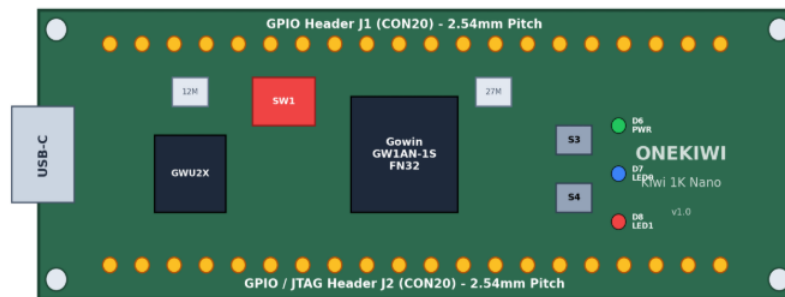


Figure 01b. FPGA 1K Kiwi Nano board layout / alternate view.

Quick Start Guide

Follow these 4 simple steps to set up your GOWIN EDA development environment and compile your first design:

- **Step 1. Registration:** Visit GOWIN Semiconductor website at www.gowinsemi.com and sign up for a user account.
- **Step 2. Download EDA Suite:** Navigate to 'Support' > 'Download GOWIN EDA' and download the correct installer matching your OS.
- **Step 3. Request License:** Select 'Apply License' on their portal, fill in your details, and GOWIN will email you a free license file.
- **Step 4. Connect and Program:** Mount the Kiwi Nano board on a breadboard, hook up the USB-C cable, set SW1 (JTAG Switch) to ON, and program using GOWIN Programmer.

System architecture and Block Diagram

The board's streamlined electrical design utilizes a single USB-C port for both power supply and JTAG programming. Integrated power management scales down the VBUS (5V) down to the logic-level 3.3V and core logic supply 1.2V.

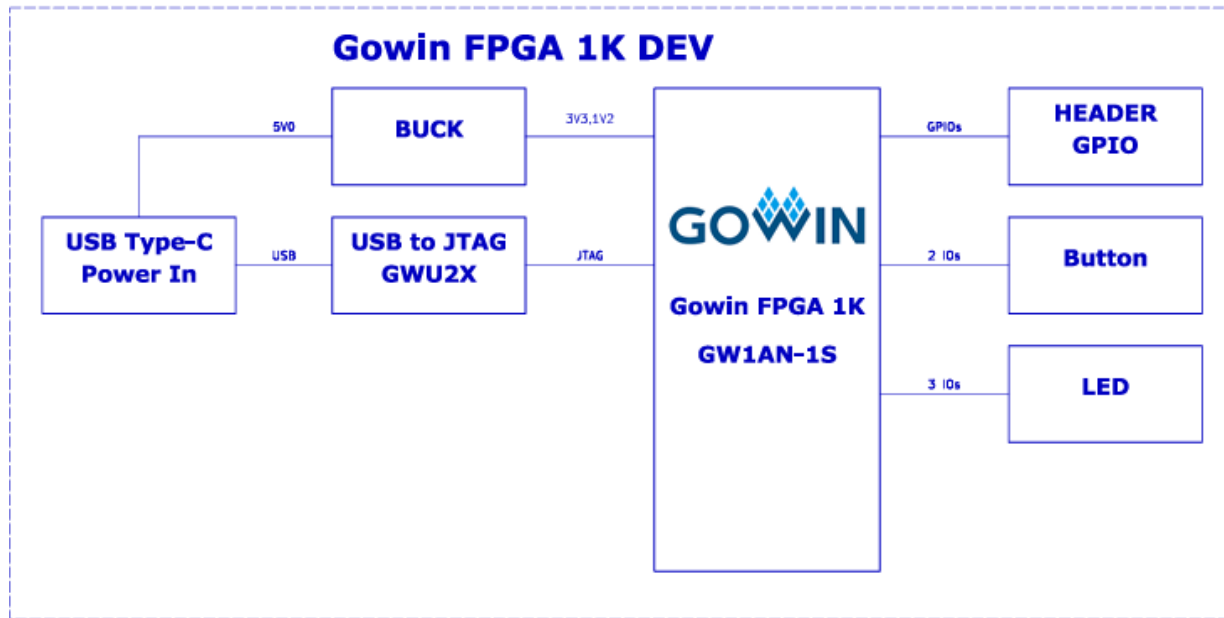


Figure 02. FPGA 1K Kiwi Nano high-level electrical system block diagram.

Onboard Control Circuitry

JTAG Mode DIP Switch (SW1)

The onboard 4-position DIP Switch (SW1) sits in-line between the debugger chip GWU2X and the FPGA JTAG port. This allows the user to disconnect the JTAG line to program external out-of-circuit systems.

Switch SW1 (All 4 Switches)	Active Mode / Signal Flow description
Switch ON	Onboard JTAG lines are routed to GW1AN-1S. Normal programming mode.
Switch OFF	Onboard JTAG is isolated. Debugger lines can be accessed on J2 headers to program external targets.

Active HIGH Status & User LEDs

The board has three onboard LEDs. **Note the active state behavior of the user LEDs (D7 and D8).** In this schematic design, the FPGA pins connect directly through current-limiting resistors to the positive terminal of the LEDs, which then terminate directly to GND. Therefore, to turn these LEDs ON, the FPGA pin must drive a Logic 1 (HIGH) output.

Designator	Associated Port / Pin	Hardware Active State	Functional Purpose
D6	Power Net (P3V3)	Always On (When Power is Active)	Indicates Board Power supply is 3.3V OK.
D7	IOR2A_LED0 (Pin 23)	Active HIGH (Glowes when logic 1)	General user LED 0, controlled by User FPGA code.
D8	IOR4B_LED1 (Pin 20)	Active HIGH (Glowes when logic 1)	General user LED 1, controlled by User FPGA code.

Debounced User Buttons (Active LOW)

Two push-buttons (S3 and S4) are wired with internal pull-up resistors to 3.3V. Pressing a button closes the circuit to ground, pulling the pin down. Hence, they operate as Active LOW.

Button	FPGA Pin	Active State	Default Status
S3 (KEY0)	IOR2B_KEY0 (Pin 22)	Active LOW (Logic 0 when pressed)	Pull-up to 3.3V (Idle Logic 1)
S4 (KEY1)	IOR4A_KEY1 (Pin 21)	Active LOW (Logic 0 when pressed)	Pull-up to 3.3V (Idle Logic 1)

Expansion GPIO Pinout Map

To facilitate rapid lab wiring, the Kiwi Nano exposes 40 expander connections through two standard headers: J2 (left) and J1 (right). Below is a direct visual guide depicting the board layout oriented vertically with the USB Type-C port facing downwards.

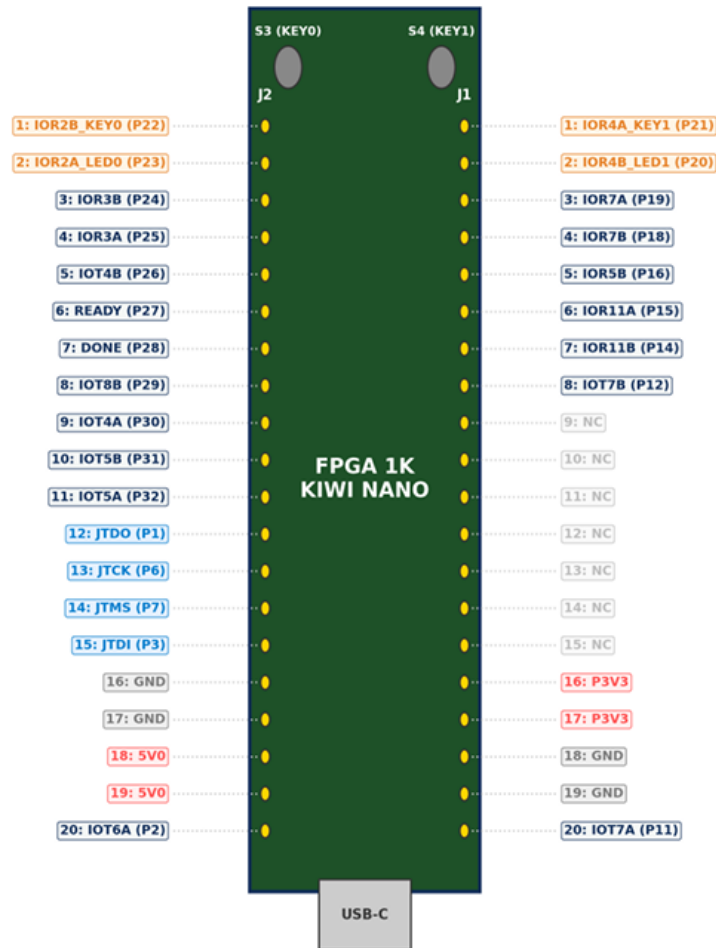


Figure 03. Expansion J1 & J2 Header vertical Pinout layout (oriented with USB-C at bottom).

Detailed Expander Pin Mapping

Table 01. Connector J2 Pin Assignment Mapping Table

Pin No.	Schematic Name	FPGA Pin	Bank	Description
1	IOR2B_KEY0	22	2	Active-LOW user button S3 (KEY0) input
2	IOR2A_LED0	23	2	Active-HIGH user LED0 (D7) output
3	IOR3B	24	2	SSPI Chip Select / General-Purpose I/O
4	IOR3A	25	2	SSPI Serial Clock / General-Purpose I/O
5	IOT4B	26	0	JTASEL_N configuration input / General-Purpose I/O
6	READY	27	1	Gowin configuration READY status pin
7	DONE	28	1	Gowin configuration DONE status pin
8	IOT8B	29	1	General-Purpose I/O
9	IOT4A	30	0	PLL high-speed input clock (PLL_T_IN) / GPIO
10	IOT5B	31	1	General-Purpose I/O
11	IOT5A	32	1	General-Purpose I/O
12	JTDO	1	0	Expander JTAG TDO signal
13	JTCK	6	0	Expander JTAG TCK signal
14	JTMS	7	0	Expander JTAG TMS signal
15	JTDI	3	0	Expander JTAG TDI signal
16, 17	GND	-	-	System ground reference rails
18, 19	5V0	-	-	VBUS power input lines directly from USB-C
20	IOT6A	2	1	RECONFIG_N initialization trigger / GPIO

Table 02. Connector J1 Pin Assignment Mapping Table

Pin No.	Schematic Name	FPGA Pin	Bank	Description
1	IOR4A_KEY1	21	2	Active-LOW user button S4 (KEY1) input
2	IOR4B_LED1	20	2	Active-HIGH user LED1 (D8) output
3	IOR7A	19	2	SPI Din input line / General-Purpose I/O
4	IOR7B	18	2	SPI Dout output line / General-Purpose I/O
5	IOR5B	16	2	Global Clock (GLCKC_2) / General-Purpose I/O
6	IOR11A	15	2	General-Purpose I/O
7	IOR11B	14	2	General-Purpose I/O
8	IOT7B	12	1	General-Purpose I/O
9 - 15	NC	-	-	Not Connected pins (isolated floating lines)
16, 17	P3V3	-	-	System 3.3V DC voltage output pins from BUCK
18, 19	GND	-	-	System ground reference rails
20	IOT7A	11	1	General-Purpose I/O

Development Board Suite

The standard retail packaging of the Kiwi 1K Nano development board suite contains the following items:

- 1x Kiwi 1K Nano FPGA Development Board
- 1x High-speed USB Type-C Cable (for programming & power)
- 2x 20-Pin 2.54mm Pitch Male Pin Headers (un-soldered for project versatility)

- 1x Protective Antistatic Cardboard Packaging Box

Customer Support and Contact: For bulk orders, technical questions, or schematic design reviews, please reach out to OneKiwi Technology Co., Ltd:

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