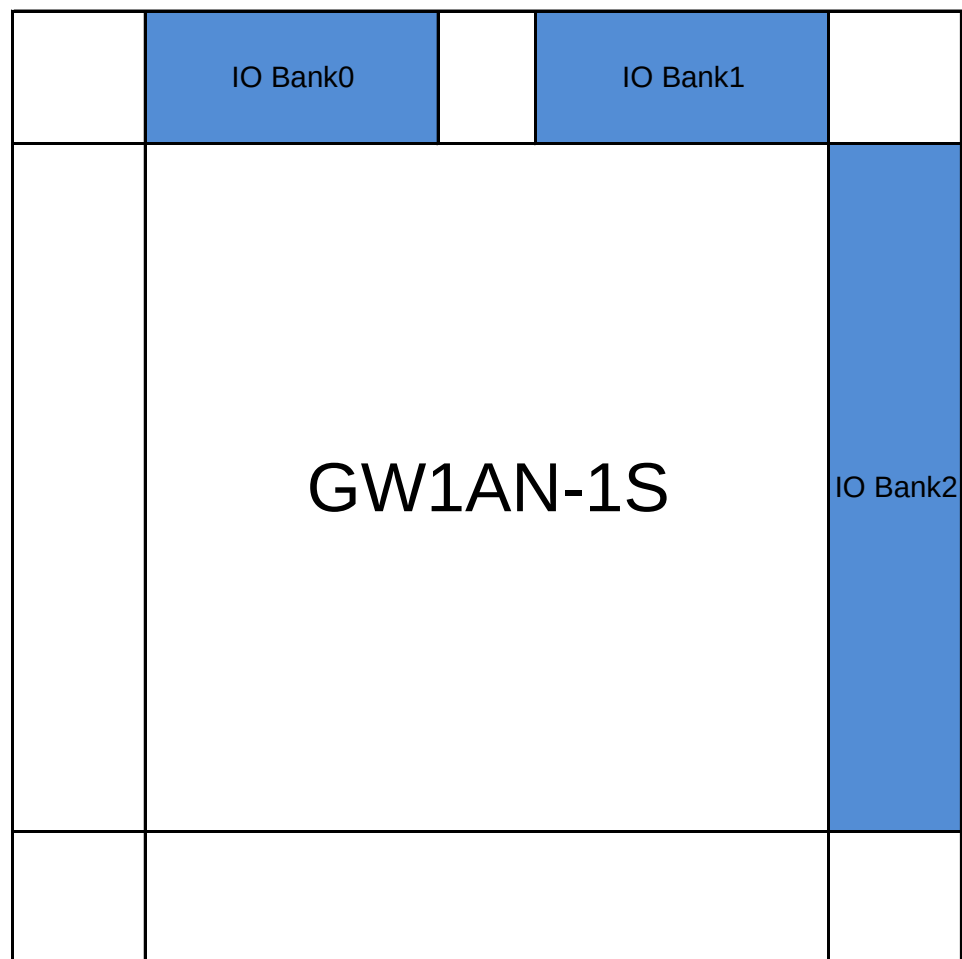


Date	Version	Description
02/13/2026	1.0E	Initial version published. FN32 package supported.

Pin Name	Direction	Description
User I/O Pins		
IO [End] [Row/Column Number] [A/B]	I/O	[End] indicates the pin location, including L(left), R(right), B(bottom), and T(top).
		[Row/Column Number] indicates the pin row/column number. If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the row number of the corresponding CFU.
		[A/B] indicates differential signal pair information.
Multi-Function Pins		
IO [End] [Row/Column Number] [A/B]/MMM		/MMM indicates one or more additional functions in addition to being general purpose user I/O. When not used for the additional functions, these pins can be user I/O.
D0	I/O	Data port D0 in CPU mode
D1	I/O	Data port D1 in CPU mode
D2	I/O	Data port D2 in CPU mode
D3	I/O	Data port D3 in CPU mode
D4	I/O	Data port D4 in CPU mode
D5	I/O	Data port D5 in CPU mode
D6	I/O	Data port D6 in CPU mode
D7	I/O	Data port D7 in CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode.0: Write;1: Read.
DOUT	O	Data output in SERIAL mode
DIN	I, internal weak pull-up	Data input in SERIAL mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode
TDO	O	Serial data output in JTAG mode
TDI	I, internal weak pull-up	Serial data input in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Reconfigure JTAG download function signal
RECONFIG_N	I, internal weak pull-up	Global reset GowinCONFIG logic signal, active low
FASTRD_N	I	Access SPI FLASH to select signal. Low, Fast Read mode; High, Read mode.
DONE ^[1]	O, internal weak pull-up	High, the programming configuration has been completed successfully; Low, the programming configuration has not been completed or failed.
	I, internal weak pull-up	When the DONE signal is low, delay the chip to activate. Activate the chip until the DONE signal is high.
READY ^[1]	I/O, internal weak pull-up	High, the device can currently be programmed and configured; Low, the device cannot be programmed and configured.
MI	I	MI in MSPI mode

Pin Name	Direction	Description
MO	O	MO in MSPI mode
MCS_N	O	Enable signal MCS_N in MSPI mode, active-low
MCLK	O	Clock output MCLK in MSPI mode, with default frequency of 2.5Mhz
SCLK	I	Clock input in SSPI, SERIAL, and CPU modes
SO	O	SO in SSPI mode
SI	I/O	SI in SSPI mode
SSPI_CS_N	I/O	Enable signal SSPI_CS_N in SSPI mode, active-low, and internal weak pull-up
CLKHOLD_N	I, internal weak pull-up	Active-high in SSPI mode; Active-low in CPU mode.
GCLKC_[x]	I	Differential input pin of GCLKT_[x], C(Comp), [x] is global clock number ^[2]
GCLKT_[x]	I	Global clock input pin, T(True), [x] is global clock number
LPLL_C_fb/RPLL_C_fb	I	Left/right PLL feedback input pin, C(Comp)
LPLL_T_fb/RPLL_T_fb	I	Left/right PLL feedback input pin, T(True)
LPLL_C_in/RPLL_C_in	I	Left/right PLL clock input pin, C(Comp)
LPLL_T_in/RPLL_T_in	I	Left/right PLL clock input pin, T(True)
MODE2	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as "VCCIO", it's internally powered; if this pin is marked as "GND", it's internally grounded.
MODE1	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as "VCCIO", it's internally powered; if this pin is marked as "GND", it's internally grounded.
MODE0	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as "VCCIO", it's internally powered; if this pin is marked as "GND", it's internally grounded.
Other Pins		
NC	NA	Reserved
VSS	NA	Ground
VCC	NA	Power supply pin of core voltage
VCCIO#	NA	Power supply pin of I/O voltage for I/O BANK#
VCCX	NA	Power supply pin of auxiliary voltage
EPAD	NA	Exposed pad. Connect to ground.
Note!		
^[1] The default state of READY/DONE is open-drain output, internal weak pull-up. DONE outputs 0 during configuration.		
^[2] When the input is single-ended, GCLKC_[x] pin is not a global clock pin.		



Note!

- [1] Each Bank has independent reference voltage (VREF).
- [2] You can select to use IOB internal VREF (equals to $0.5 \times VCCIO$).
- [3] You can also select to use external VREF input (use any IO pins as external VREF input).

Name	Description	Min.	Max.
VCC	LV version core voltage	1.14V	1.26V
VCCIO	I/O Bank power supply voltage	1.14V	3.6V

Note !						
[1] LV version						
Pin Name	Function	BANK	Configuration Function	Differential Pair	X16	FN32 ^[1]
IOT2A/TMS	I/O	0	TMS	True_of_IOT2B	x16	7
IOT2B/TCK	I/O	0	TCK	Comp_of_IOT2A	none	6
IOT3A/TDI	I/O	0	TDI	True_of_IOT3B	none	3
IOT3B/TDO	I/O	0	TDO	Comp_of_IOT3A	none	1
IOT4A/PLL_T_IN	I/O	0	PLL_T_IN	True_of_IOT4B	none	30
IOT4B/JTAGSEL_N	I/O	0	JTAGSEL_N	Comp_of_IOT4A	none	26
IOT5A	I/O	1		True_of_IOT5B	x16	32
IOT5B	I/O	1		Comp_of_IOT5A	none	31
IOT6A/RECONFIG_N	I/O	1	RECONFIG_N	True_of_IOT6B	none	2
IOT6B/DONE	I/O	1	DONE	Comp_of_IOT6A	none	28
IOT7A	I/O	1		True_of_IOT7B	x16	11
IOT7B	I/O	1		Comp_of_IOT7A	none	12
IOT8A/READY	I/O	1	READY	True_of_IOT8B	none	27
IOT8B	I/O	1		Comp_of_IOT8A	none	29
IOR2A	I/O	2		True_of_IOR2B	x16	23
IOR2B	I/O	2		Comp_of_IOR2A	none	22
IOR3A/SCLK	I/O	2	SCLK	True_of_IOR3B	none	25
IOR3B/SSPI_CS_N/D0	I/O	2	SSPI_CS_N/D0	Comp_of_IOR3A	none	24
IOR4A/SI/D2	I/O	2	SI/D2	True_of_IOR4B	x16	21
IOR4B/SO/D1	I/O	2	SO/D1	Comp_of_IOR4A	none	20
IOR5A/GCLKT_2	I/O	2	GCLKT_2	True_of_IOR5B	none	17
IOR5B/GCLKC_2	I/O	2	GCLKC_2	Comp_of_IOR5A	none	16
IOR7A/GCLKT_3/DIN/CLKHOLD_N	I/O	2	GCLKT_3/DIN/CLKHOLD_N	True_of_IOR7B	x16	19
IOR7B/GCLKC_3/DOOUT/WE_N	I/O	2	GCLKC_3/DOOUT/WE_N	Comp_of_IOR7A	none	18
IOR11A	I/O	2		True_of_IOR11B	x16	15
IOR11B	I/O	2		Comp_of_IOR11A	none	14
VCCIO0	Power	N/A				5
VCCIO1	Power	N/A				4

Note ! [1] LV version						
Pin Name	Function	BANK	Configuration Function	Differential Pair	X16	FN32 ^[1]
VCCIO2	Power	N/A				13
VCC/VCCPLL	Power	N/A				9
VSS	Ground	N/A				8
VSS	Ground	N/A				10