



GW1AN series of FPGA Products **Package & Pinout User Guide**

UG188-1.1E, 02/13/2026

Preliminary

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Preliminary

Revision History

Date	Version	Description
12/30/2025	1.0E	Initial version published.
02/13/2026	1.1E	● The information of FN32 package for GW1AN-1S devices added. ● The information of LQ100X/LQ144X/PG256X/UG256X packages for GW1AN-5 devices added.

Contents

Contents	i
List of Figures	iii
List of Tables	iv
1 About This Guide	1
1.1 Purpose	1
1.2 Related Documents	1
1.3 Terminology and Abbreviations	1
1.4 Support and Feedback	2
2 Overview	3
2.1 PB-Free Package	3
2.2 Package, Max. User I/O, and LVDS Pair Information	3
2.3 Power Pin	4
2.4 Pin Quantity	4
2.4.1 Quantity of GW1AN-1 Pins	4
2.4.2 Quantity of GW1AN-1S Pins	5
2.4.3 Quantity of GW1AN-5 Pins	6
2.5 I/O BANK Introduction	8
3 View of Pin Distribution	9
3.1 View of GW1AN-1 Pin Distribution	9
3.1.1 View of QN48 (LV Version) Pin Distribution	9
3.2 View of GW1AN-1S Pin Distribution	10
3.2.1 View of FN32 (LV Version) Pin Distribution	10
3.3 View of GW1AN-5 Pin Distribution	10
3.3.1 View of LQ100X (LV Version) Pin Distribution	10
3.3.2 View of LQ100X (UV Version) Pin Distribution	11
3.3.3 View of LQ144X (LV Version) Pin Distribution	12
3.3.4 View of LQ144X (UV Version) Pin Distribution	13
3.3.5 View of PG256X (LV Version) Pin Distribution	14
3.3.6 View of PG256X (UV Version) Pin Distribution	15
3.3.7 View of UG256X (LV Version) Pin Distribution	16

3.3.8 View of UG256X (UV Version) Pin Distribution	17
4 Package Diagram.....	18
4.1 FN32 Package Outline (4mm x 4mm, GW1AN-1S)	18
4.2 QN48 Package Outline (6mm x 6mm, GW1AN-1).....	20
4.3 LQ100X Package Outline (14mm x 14mm, GW1AN-5)	22
4.4 LQ144X Package Outline (20mm x 20mm, GW1AN-5)	24
4.5 PG256X Package Outline (17mm x 17mm, GW1AN-5).....	26
4.6 UG256X Package Outline (14mm x 14mm, GW1AN-5).....	28

List of Figures

Figure 3-1 View of GW1AN-1 QN48 (LV Version) Pin Distribution (Top View)	9
Figure 3-2 View of GW1AN-1S FN32 (LV Version) Pin Distribution (Top View)	10
Figure 3-3 View of GW1AN-5 LQ100X (LV Version) Pin Distribution (Top View)	10
Figure 3-4 View of GW1AN-5 LQ100X (UV Version) Pin Distribution (Top View)	11
Figure 3-5 View of GW1AN-5 LQ144X (LV Version) Pin Distribution (Top View)	12
Figure 3-6 View of GW1AN-5 LQ144X (UV Version) Pin Distribution (Top View)	13
Figure 3-7 View of GW1AN-5 PG256X (LV Version) Pin Distribution (Top View)	14
Figure 3-8 View of GW1AN-5 PG256X (UV Version) Pin Distribution (Top View)	15
Figure 3-9 View of GW1AN-5 UG256X (LV Version) Pin Distribution (Top View)	16
Figure 3-10 View of GW1AN-5 UG256X (UV Version) Pin Distribution (Top View)	17
Figure 4-1 Package Outline FN32	18
Figure 4-2 Recommended PCB Layout FN32	19
Figure 4-3 Package Outline QN48	20
Figure 4-4 Recommended PCB Layout QN48	21
Figure 4-5 Package Outline LQ100X	22
Figure 4-6 Recommended PCB Layout LQ100X	23
Figure 4-7 Package Outline LQ144X	24
Figure 4-8 Recommended PCB Layout LQ144X	25
Figure 4-9 Package Outline PG256X	26
Figure 4-10 Recommended PCB Layout PG256X	27
Figure 4-11 Package Outline UG256X	28
Figure 4-12 Recommended PCB Layout UG256X	29

List of Tables

Table 1-1 Terminology and Abbreviations	1
Table 2-1 Package, Max. User I/O, and LVDS Pair Information	3
Table 2-2 Power Pins of GW1AN.....	4
Table 2-3 Quantity of GW1AN-1 Pins	4
Table 2-4 Quantity of GW1AN-1S Pins	5
Table 3-1 Other Pins of GW1AN-1 QN48 (LV Version).....	9
Table 3-2 Other Pins of GW1AN-1 FN32 (LV Version)	10
Table 3-3 Other Pins of GW1AN-5 LQ100X (LV Version).....	11
Table 3-4 Other Pins of GW1AN-5 LQ100X (UV Version).....	11
Table 3-5 Other Pins of GW1AN-5 LQ144X (LV Version).....	12
Table 3-6 Other Pins of GW1AN-5 LQ144X (UV Version).....	13
Table 3-7 Other Pins of GW1AN-5 PG256X (LV Version)	14
Table 3-8 Other Pins of GW1AN-5 PG256X (UV Version)	15
Table 3-9 Other Pins of GW1AN-5 UG256X (LV Version)	16
Table 3-10 Other Pins of GW1AN-5 UG256X (UV Version)	17

1 About This Guide

1.1 Purpose

This manual introduces the Gowin GW1AN series of FPGA products packages and provides pin definitions, lists of pin numbers, pin distribution views, and package diagrams.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- [DS186, GW1AN-1S & 1 Data Sheet](#)
- [UG187, GW1AN-1 Pinout](#)
- [UG194, GW1AN-1S Pinout](#)
- [UG196, GW1AN-3 & 5 Pinout](#)
- [UG192, GW1AN-5 Pinout](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FN	QFN Package
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
LQ	LQFP Package
PG	PBGA Package
QN	QFN Package
UG	UBGA Package

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

The GW1AN series of FPGA Products are the 1 series products of GOWINSEMI Arora family. They are available in various forms that offer high I/O compatibility and flexible usage.

2.1 PB-Free Package

The GW1AN series of FPGA products are PB free in line with the EU ROHS environmental directives. The substances used in the GW1AN series of FPGA products are in full compliance with the IPC-1752 standards.

2.2 Package, Max. User I/O, and LVDS Pair Information

Table 2-1 Package, Max. User I/O, and LVDS Pair Information

Package	Pitch (mm)	Size (mm)	E-pad Size (mm)	GW1AN-1	GW1AN-1S	GW1AN-5
FN32	0.4	4 x 4	2.7 x 2.7	-	26	-
QN48	0.4	6 x 6	4.2 x 4.2	41	-	-
LQ100X	0.5	14 x 14		-	-	81(4)
LQ144X	0.5	20 x 20		-	-	116(9)
PG256X	1.0	17 x 17		-	-	208(12)
UG256X	0.8	14 x 14		-	-	208(12)

Note!

- In this manual, abbreviations are employed to refer to the package types. See 1.3 Terminology and Abbreviations.
- See GW1AN series Pinouts for further details.
- The JTAGSEL_N pin and the four pins of JTAG (TCK, TDI, TDO, and TMS) cannot be simultaneously used as I/O. When mode [2:0] = 001, JTAGSEL_N and the four JTAG pins (TCK, TDI, TDO, and TMS) can be used as GPIO simultaneously.

2.3 Power Pin

Table 2-2 Power Pins of GW1AN

VCC	VCCIO0	VCCIO1	VCCIO2
VCCIO3	VCCIO4	VCCIO5	VSS
VCCX	VCCADC0	VCCADC1	VCC/VCCPLL

2.4 Pin Quantity

2.4.1 Quantity of GW1AN-1 Pins

Table 2-3 Quantity of GW1AN-1 Pins

Pin type		GW1AN-1
		QN48
Single-ended I/O/Differential pair ^[1]	BANK0	11
	BANK1	9
	BANK2	12
	BANK3	9
Max. User I/O ^[2]		41
VCC		2
VCCIO1		1
VCCIO2		1
VCCIO0/VCCIO3 ^[3]		1
VSS		2
MODE0		0
MODE1		0
MODE2		0
JTAGSEL_N		0

Note!

- ^[1] Quantity of single-ended/differential I/Os include CLK pins, and download pins.
- ^[2] The JTAGSEL_N and JTAG pins are exclusive. The JTAGSEL_N pin and the four pins of JTAG (TCK, TDI, TDO, and TMS) cannot be simultaneously used as I/O.
- ^[3] Pin Multiplexing.

2.4.2 Quantity of GW1AN-1S Pins

Table 2-4 Quantity of GW1AN-1S Pins

Pin type		GW1AN-1S
		FN32
Single-ended I/O/Differential pair ^[1]	BANK0	6/3/0
	BANK1	8/4/0
	BANK2	12/6/0
Max. User I/O ^[2]		26
VCC/VCCPLL ^[3]		1
VCCIO0		1
VCCIO1		1
VCCIO2		1
VSS		2
MODE0		0
MODE1		0
MODE2		0
JTAGSEL_N		1

Note!

- ^[1] Quantity of single-ended/differential I/Os include CLK pins, and download pins.
- ^[2] The JTAGSEL_N and JTAG pins are exclusive. The JTAGSEL_N pin and the four pins of JTAG (TCK, TDI, TDO, and TMS) cannot be simultaneously used as I/O.
- ^[3] Pin Multiplexing.

2.4.3 Quantity of GW1AN-5 Pins

Pin type		GW1AN-5							
		LQ100X ^[4]	LQ100X ^[5]	LQ144X ^[4]	LQ144X ^[5]	PG256X ^[4]	PG256X ^[5]	UG256X ^[4]	UG256X ^[5]
Single-ended I/O/Differential pair ^[1]	BANK0	20	20	29	29	52	52	52	52
	BANK1	21	21	29	29	52	52	52	52
	BANK2	20	20	29	29	52	52	52	52
	BANK3	6	6	9	9	16	16	16	16
	BANK4	6	6	10	10	16	16	16	16
	BANK5	8	8	10	10	20	20	20	20
Max. User I/O ^[2]		81	81	116	116	208	208	208	208
Differential Pair		4	4	9	9	12	12	12	12
VCC		2	0	4	0	8	0	8	0
VCCX		0	2	0	4	0	8	0	8
VCCIO0		0	2	0	3	0	4	0	4
VCCIO1		2	2	3	3	4	4	4	4
VCCIO2		2	2	3	3	4	4	4	4
VCCIO3		1	1	1	1	0	0	0	0
VCCIO4		1	1	1	1	2	2	2	2
VCCIO5		1	1	1	1	1	1	1	1
VCCIO0/VCCX ^[3]		2	0	3	0	4	0	4	0
VCCIO3/VCCADC0/VCCADC1 ^[3]		0	0	0	0	1	1	1	1
VSS		8	8	12	12	24	24	24	24
MODE0		0	0	0	0	0	0	0	0
MODE1		0	0	0	0	0	0	0	0
MODE2		0	0	0	0	0	0	0	0

Pin type	GW1AN-5							
	LQ100X ^[4]	LQ100X ^[5]	LQ144X ^[4]	LQ144X ^[5]	PG256X ^[4]	PG256X ^[5]	UG256X ^[4]	UG256X ^[5]
JTAGSEL_N	1	1	1	1	1	1	1	1

Note!

- ^[1] Quantity of single-ended/differential I/Os include CLK pins, and download pins.
- ^[2] The JTAGSEL_N and JTAG pins are exclusive. The JTAGSEL_N pin and the four pins of JTAG (TCK, TDI, TDO, and TMS) cannot be simultaneously used as I/O.
- ^[3] Pin Multiplexing.
- ^[4] LV version.
- ^[5] UV version.

2.5 I/O BANK Introduction

GW1AN-1 includes four I/O banks.

GW1AN-1S includes three I/O banks.

Please refer to [DS186, GW1AN-1S & 1 Data Sheet > 2.4 Input/Output Blocks](#) for further details.

GW1AN-5 includes six banks.

Please refer to [DS196, GW1AN-3 & 5 Data Sheet > 2.4 Input/Output Blocks](#) for further details.

This manual provides an overview of the distribution view of the pins in the GW1AN series of FPGA products. For details, please refer to [3 View of Pin Distribution](#). The I/O Banks in GW1AN series of FPGA products are marked with different colors.

The User I/O, power, and ground are also marked with different symbols and colors. The various symbols and colors used for the various pins are defined as follows:

-  denotes I/Os in BANK0.
-  denotes I/Os in BANK1.
-  denotes I/Os in BANK2.
-  denotes I/Os in BANK3.
-  denotes I/Os in BANK4.
-  denotes I/Os in BANK5.
-  denotes VCC, VCCX, and VCCIO.
-  indicates VSS.

3 View of Pin Distribution

3.1 View of GW1AN-1 Pin Distribution

3.1.1 View of QN48 (LV Version) Pin Distribution

Figure 3-1 View of GW1AN-1 QN48 (LV Version) Pin Distribution (Top View)

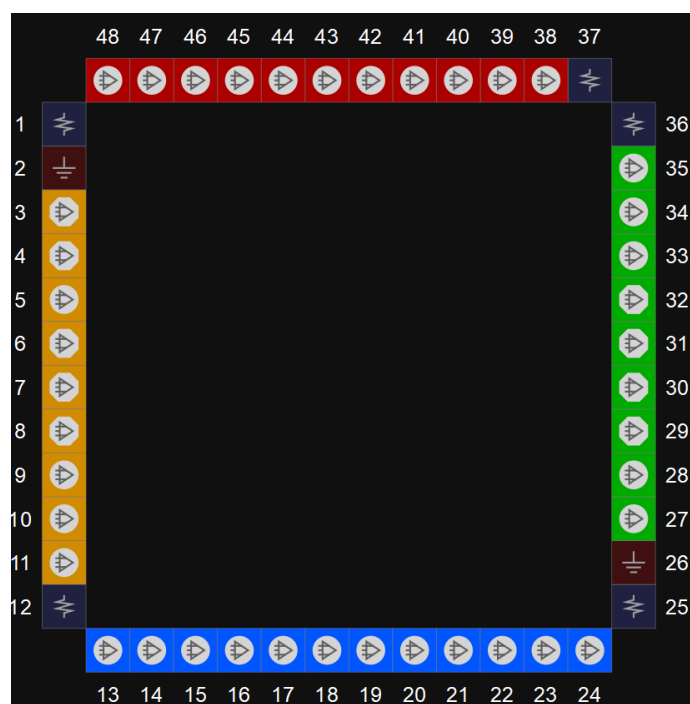


Table 3-1 Other Pins of GW1AN-1 QN48 (LV Version)

VCC	12, 37
VCCIO1	36
VCCIO2	25
VCCIO0/VCCIO3	1
VSS	2, 26

3.2 View of GW1AN-1S Pin Distribution

3.2.1 View of FN32 (LV Version) Pin Distribution

Figure 3-2 View of GW1AN-1S FN32 (LV Version) Pin Distribution (Top View)

TBD

Table 3-2 Other Pins of GW1AN-1 FN32 (LV Version)

VCC/VCCPLL	9
VCCIO0	5
VCCIO1	4
VCCIO2	13
VSS	8,10

3.3 View of GW1AN-5 Pin Distribution

3.3.1 View of LQ100X (LV Version) Pin Distribution

Figure 3-3 View of GW1AN-5 LQ100X (LV Version) Pin Distribution (Top View)

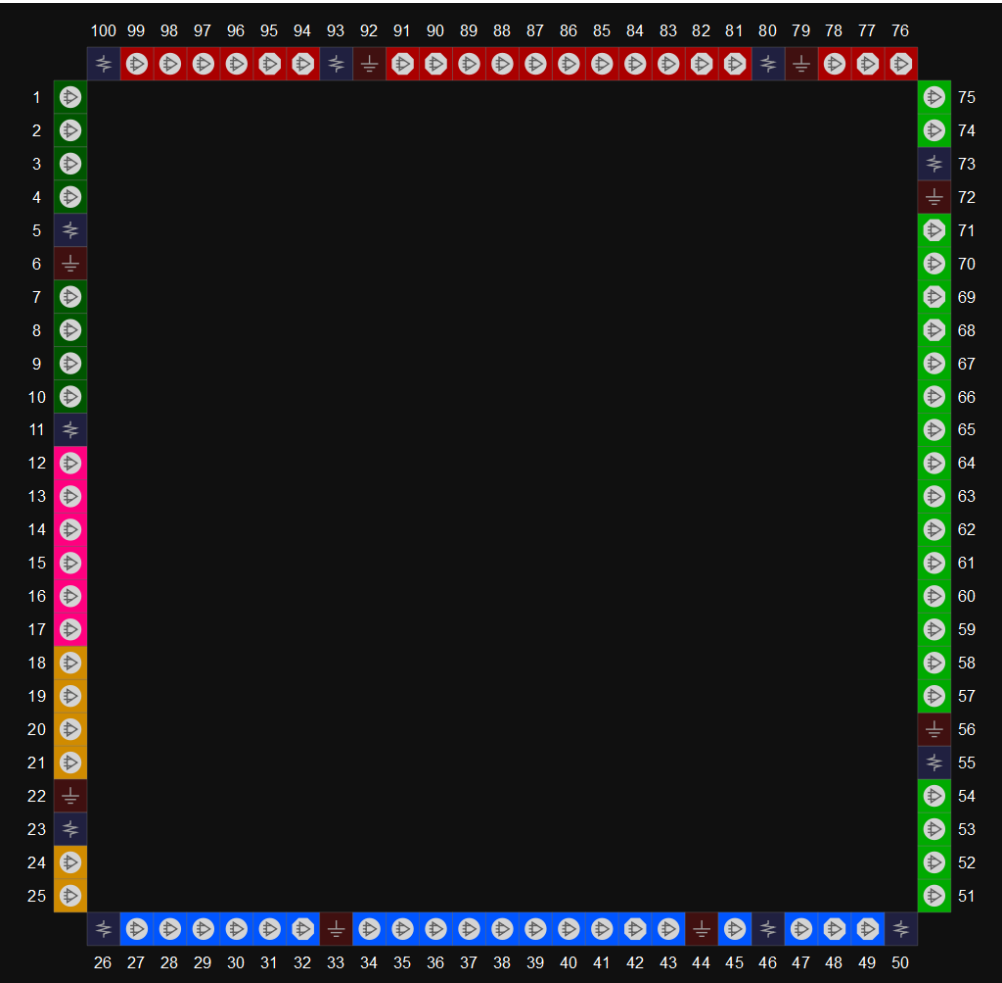


Table 3-3 Other Pins of GW1AN-5 LQ100X (LV Version)

VCC	50,100
VCCIO1	55, 73
VCCIO2	26, 46
VCCIO3	23
VCCIO4	11
VCCIO5	5
VCCIO0/VCCX	80, 93
VSS	6, 22, 33, 44, 56, 72, 79, 92

3.3.2 View of LQ100X (UV Version) Pin Distribution

Figure 3-4 View of GW1AN-5 LQ100X (UV Version) Pin Distribution (Top View)

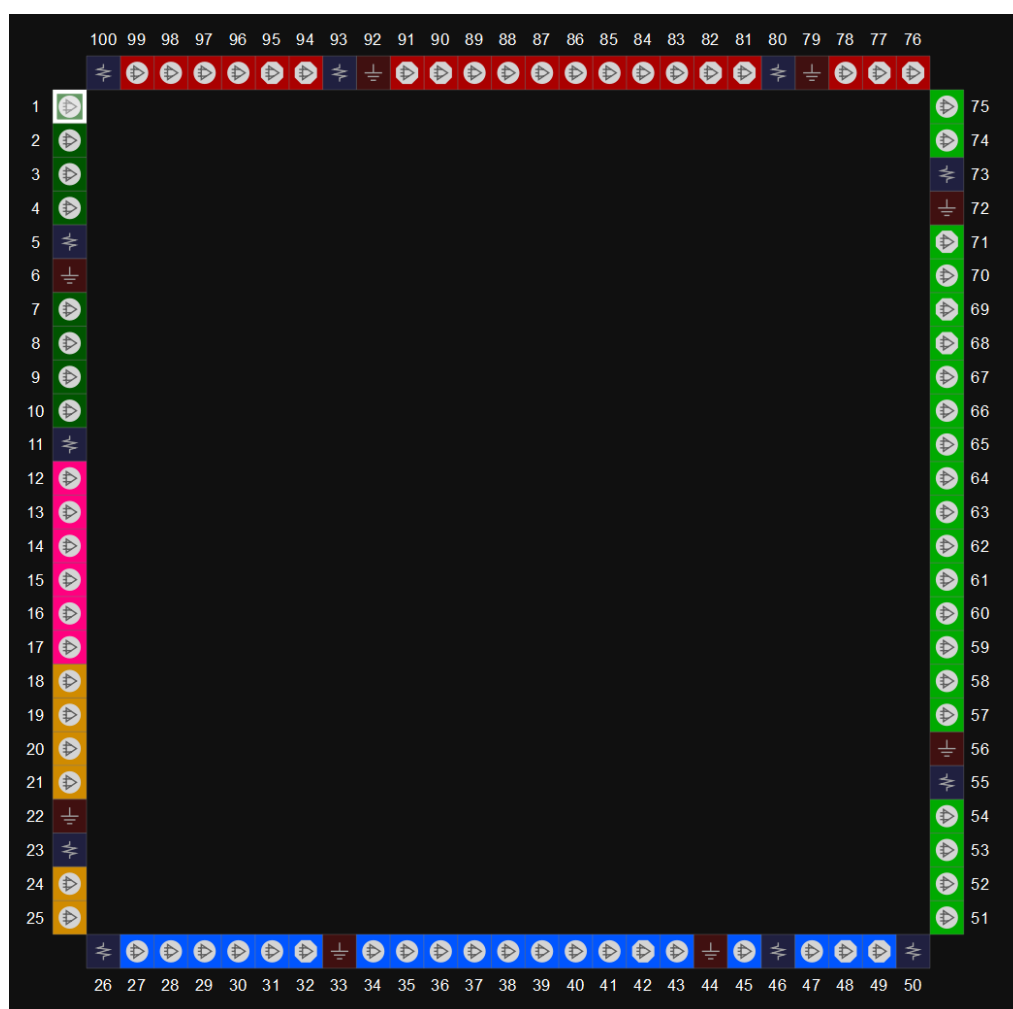


Table 3-4 Other Pins of GW1AN-5 LQ100X (UV Version)

VCCX	50,100
VCCIO0	80, 93
VCCIO1	55, 73
VCCIO2	26, 46

VCCIO3	23
VCCIO4	11
VCCIO5	5
VSS	6, 22, 33, 44, 56, 72, 79, 92

3.3.3 View of LQ144X (LV Version) Pin Distribution

Figure 3-5 View of GW1AN-5 LQ144X (LV Version) Pin Distribution (Top View)

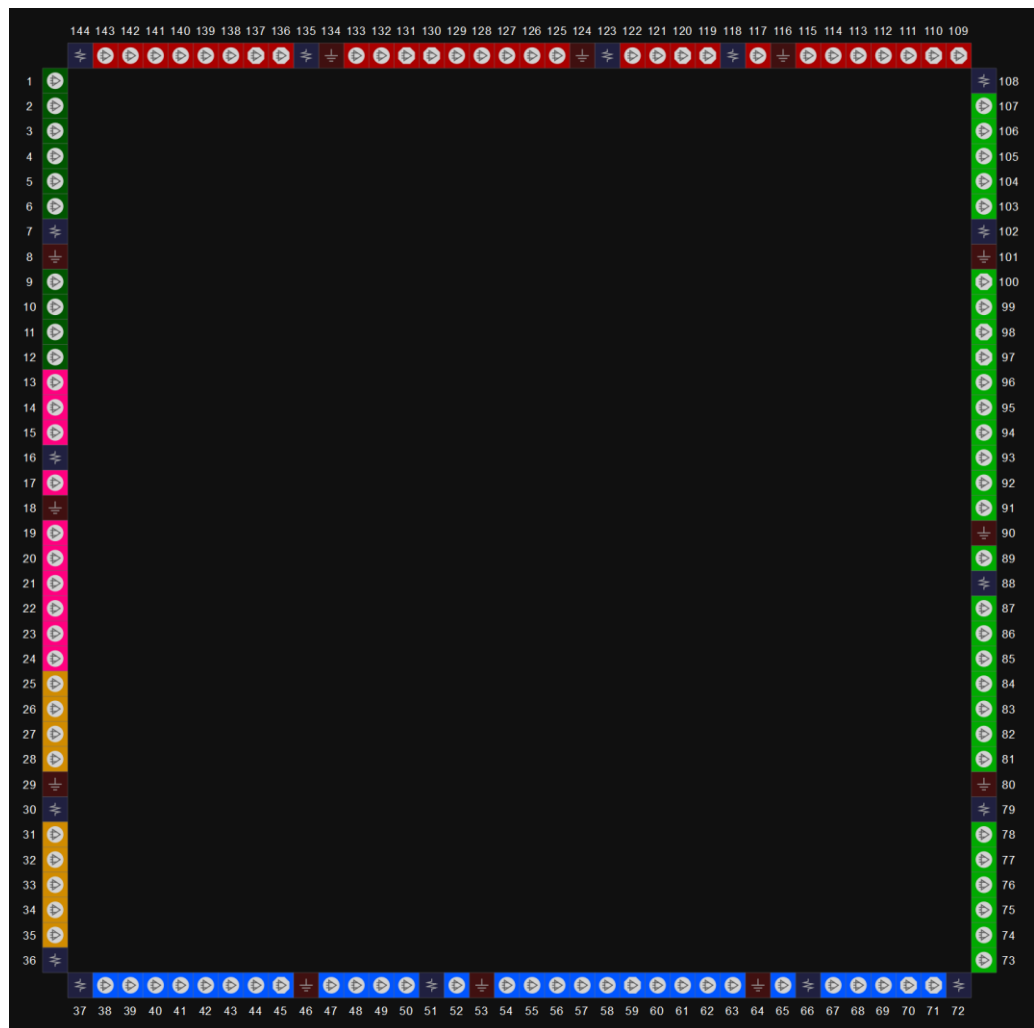


Table 3-5 Other Pins of GW1AN-5 LQ144X (LV Version)

VCC	36, 72, 108, 144
VCCIO1	79, 88, 102
VCCIO2	37, 51, 66
VCCIO3	30
VCCIO4	16
VCCIO5	7
VCCIO0/VCCX	118, 123, 135
VSS	8, 18, 29, 46, 53, 64, 80, 90, 101, 116, 124, 134

3.3.4 View of LQ144X (UV Version) Pin Distribution

Figure 3-6 View of GW1AN-5 LQ144X (UV Version) Pin Distribution (Top View)

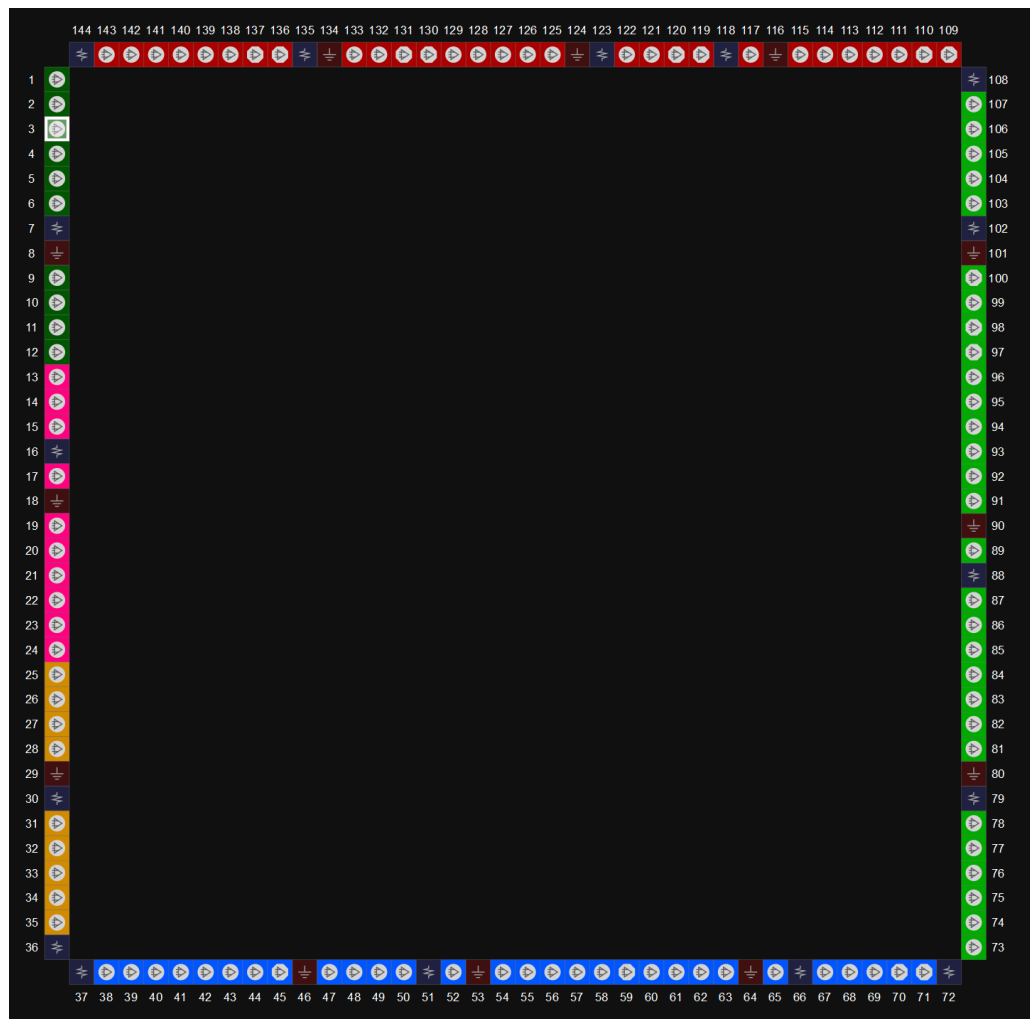


Table 3-6 Other Pins of GW1AN-5 LQ144X (UV Version)

VCCX	36,72,108,144
VCCIO0	118,123,135
VCCIO1	79, 88, 102
VCCIO2	37, 51, 66
VCCIO3	30
VCCIO4	16
VCCIO5	7
VSS	8, 18, 29, 46, 53, 64, 80, 90, 101, 116, 124, 134

3.3.5 View of PG256X (LV Version) Pin Distribution

Figure 3-7 View of GW1AN-5 PG256X (LV Version) Pin Distribution (Top View)

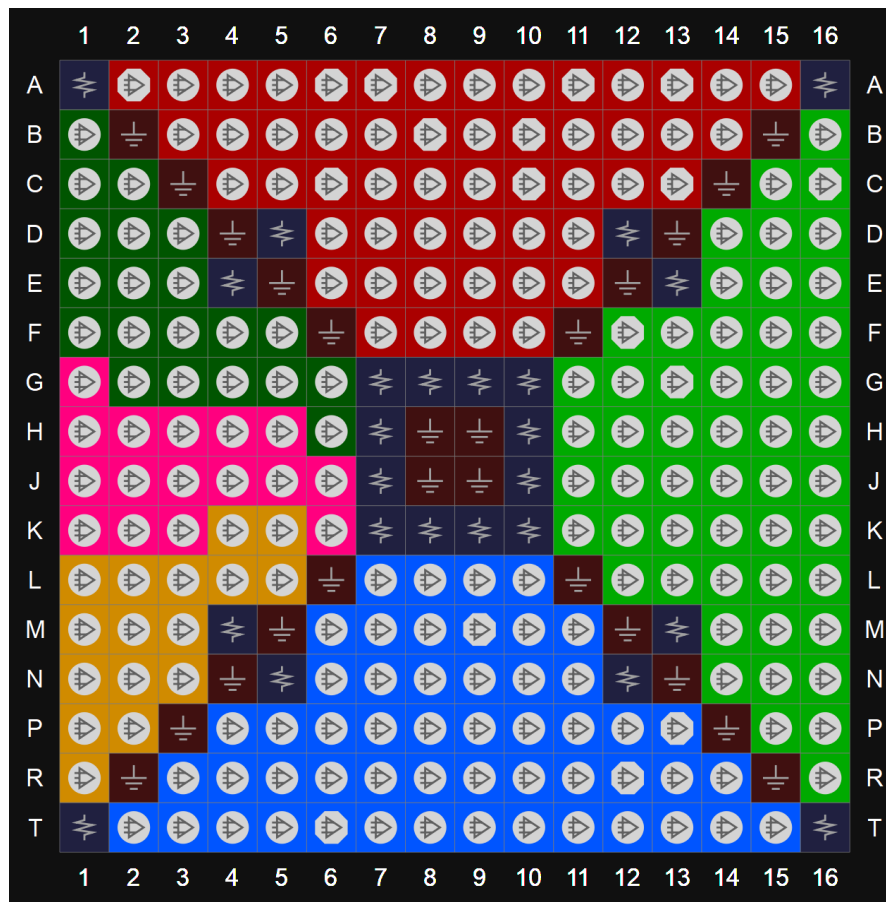


Table 3-7 Other Pins of GW1AN-5 PG256X (LV Version)

VCC	A1,A16,G10,K7,T1,T16,G7,K10
VCCIO1	M13,J10,E13,H10
VCCIO2	N5,K9,N12,K8
VCCIO4	H7,J7
VCCIO5	E4
VCCIO0/VCCX	D12,D5,G9,G8
VCCIO3/VCCADC0/VCCADC1	M4
VSS	M12,M5,N13,N4,P14,P3,R15,R2,B2,B15,C3,C14,D4,D13,E5,E12,F6,F11,H8,H9,J8,J9,L6,L11

3.3.6 View of PG256X (UV Version) Pin Distribution

Figure 3-8 View of GW1AN-5 PG256X (UV Version) Pin Distribution (Top View)

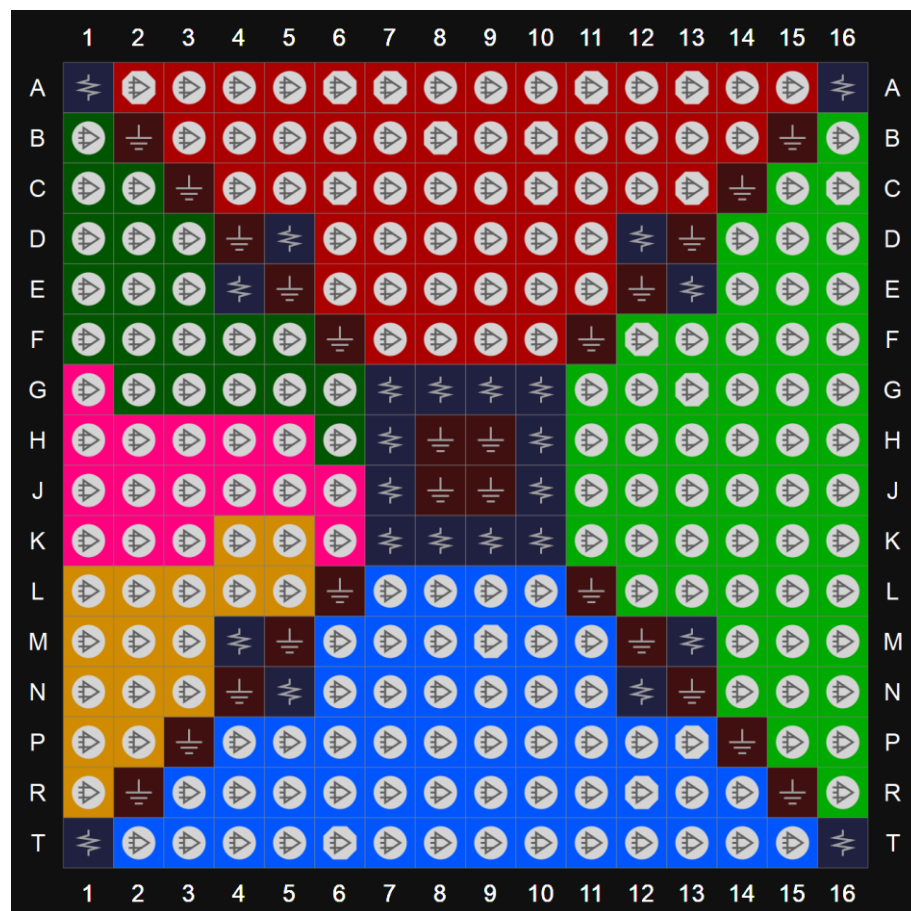


Table 3-8 Other Pins of GW1AN-5 PG256X (UV Version)

VCCX	A1,A16,G10,K7,T1,T16,G7,K10
VCCIO0	D12,D5,G9,G8
VCCIO1	M13,J10,E13,H10
VCCIO2	N5,K9,N12,K8
VCCIO4	H7,J7
VCCIO5	E4
VCCIO3/VCCADC0/VCCADC1	M4
VSS	M12,M5,N13,N4,P14,P3,R15,R2,B2,B15,C3,C14,D4,D13,E5,E12,F6,F11,H8,H9,J8,J9,L6,L11

3.3.7 View of UG256X (LV Version) Pin Distribution

Figure 3-9 View of GW1AN-5 UG256X (LV Version) Pin Distribution (Top View)

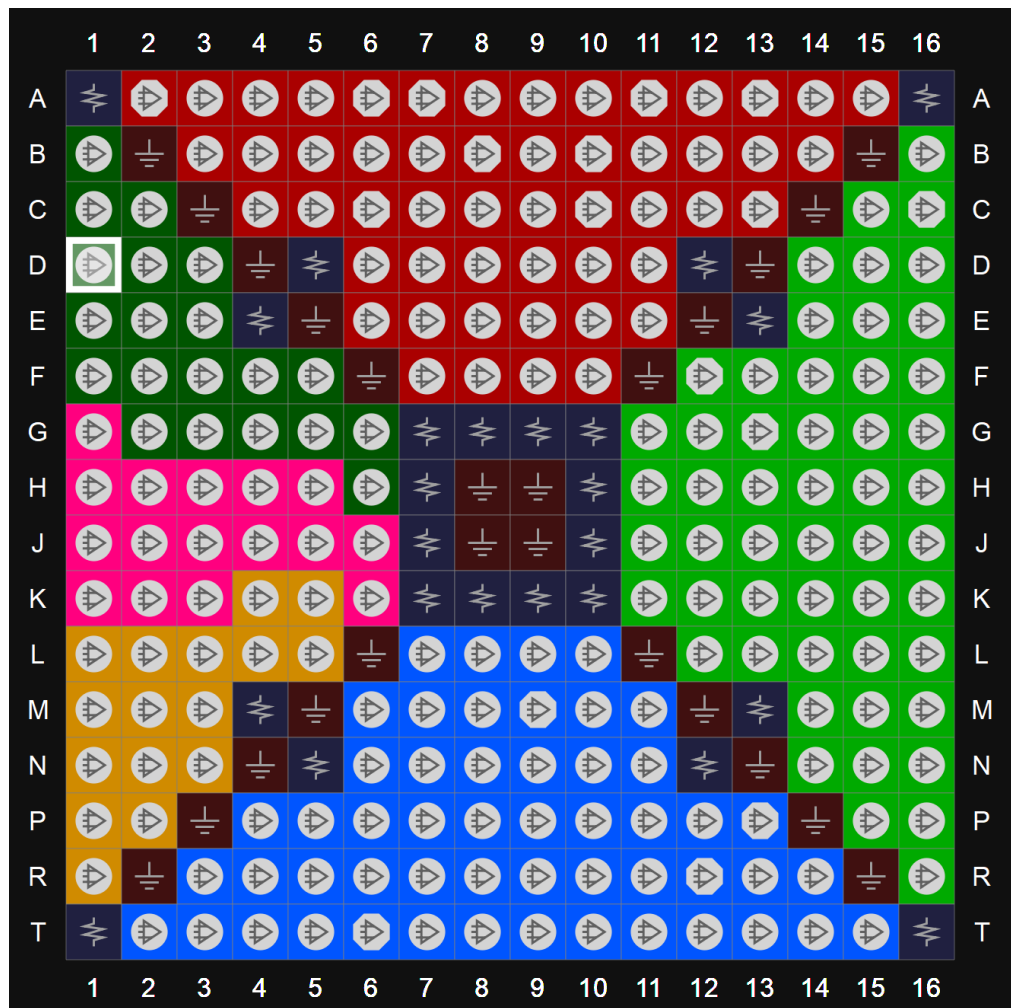


Table 3-9 Other Pins of GW1AN-5 UG256X (LV Version)

VCC	A1,A16,G10,K7,T1,T16,G7,K10
VCCIO1	M13,J10,E13,H10
VCCIO2	N5,K9,N12,K8
VCCIO4	H7,J7
VCCIO5	E4
VCCIO0/VCCX	D12,D5,G9,G8
VCCIO3/VCCADC0/VCCADC1	M4
VSS	M12,M5,N13,N4,P14,P3,R15,R2,B2,B15,C3,C14,D4,D13,E5,E12,F6,F11,H8,H9,J8,J9,L6,L11

3.3.8 View of UG256X (UV Version) Pin Distribution

Figure 3-10 View of GW1AN-5 UG256X (UV Version) Pin Distribution (Top View)

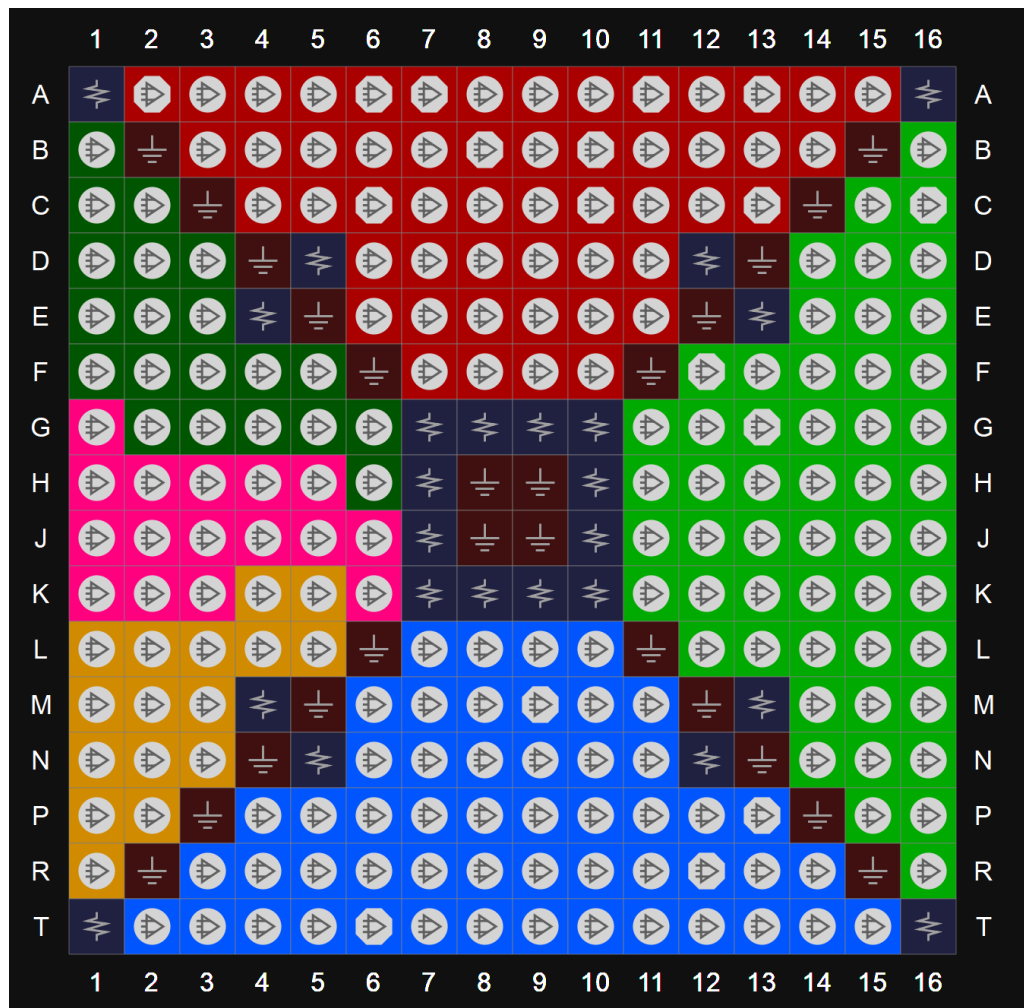


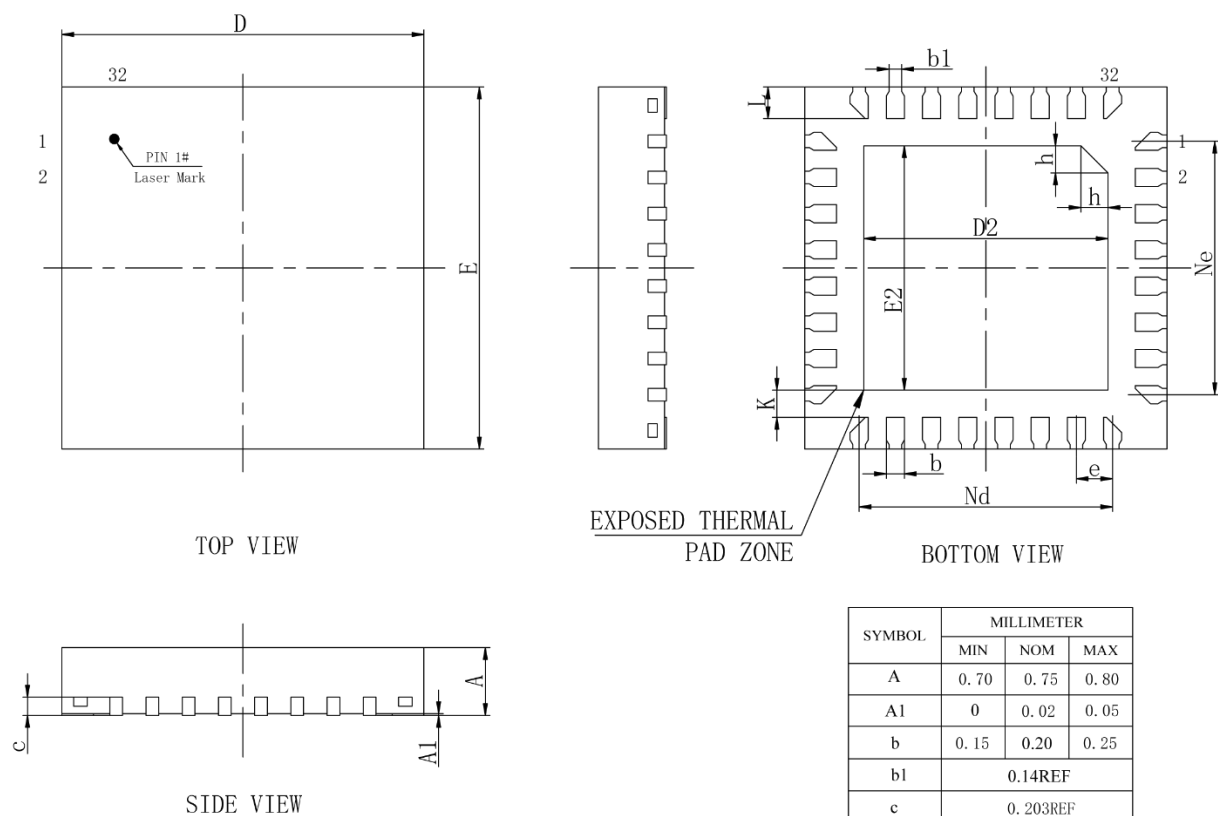
Table 3-10 Other Pins of GW1AN-5 UG256X (UV Version)

VCCX	A1,A16,G10,K7,T1,T16,G7,K10
VCCIO0	D12,D5,G9,G8
VCCIO1	M13,J10,E13,H10
VCCIO2	N5,K9,N12,K8
VCCIO4	H7,J7
VCCIO5	E4
VCCIO3/VCCADC0/VCCADC1	M4
VSS	M12,M5,N13,N4,P14,P3,R15,R2,B2,B15,C3,C14,D4,D13,E5,E12,F6,F11,H8,H9,J8,J9,L6,L11

4 Package Diagram

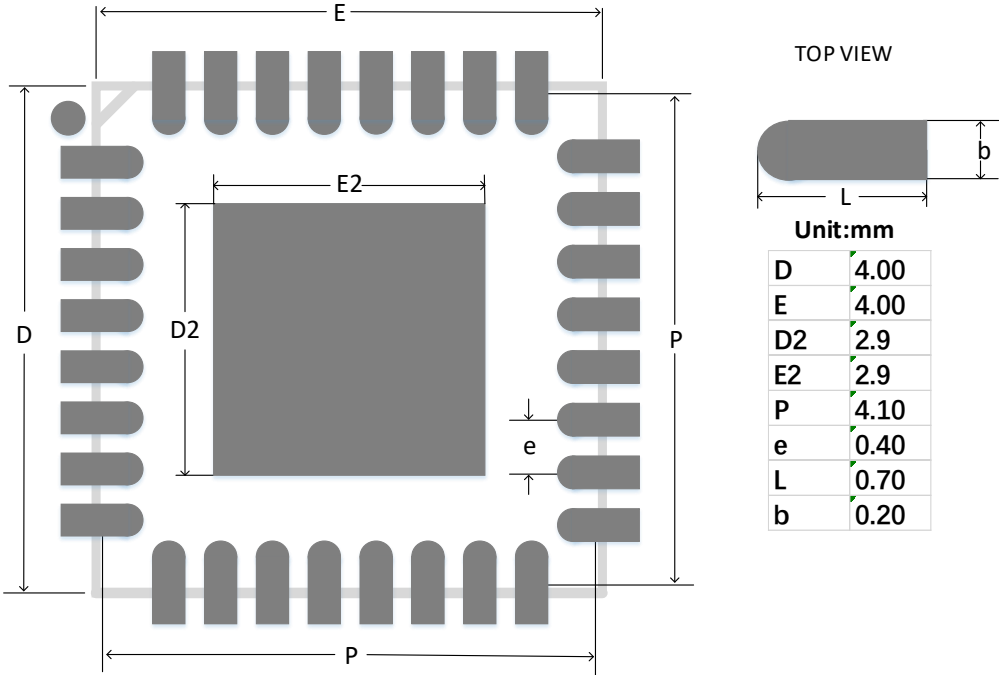
4.1 FN32 Package Outline (4mm x 4mm, GW1AN-1S)

Figure 4-1 Package Outline FN32



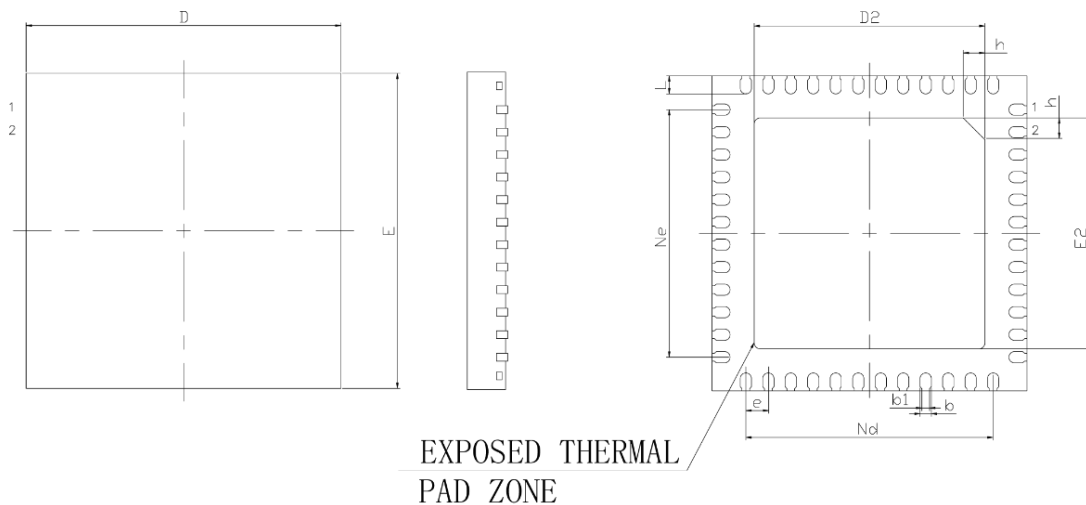
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.203REF		
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
Ne	2.80BSC		
L	0.30	0.35	0.40
h	0.25	0.30	0.35
K	0.30REF		

Figure 4-2 Recommended PCB Layout FN32

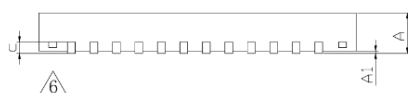


4.2 QN48 Package Outline (6mm x 6mm, GW1AN-1)

Figure 4-3 Package Outline QN48

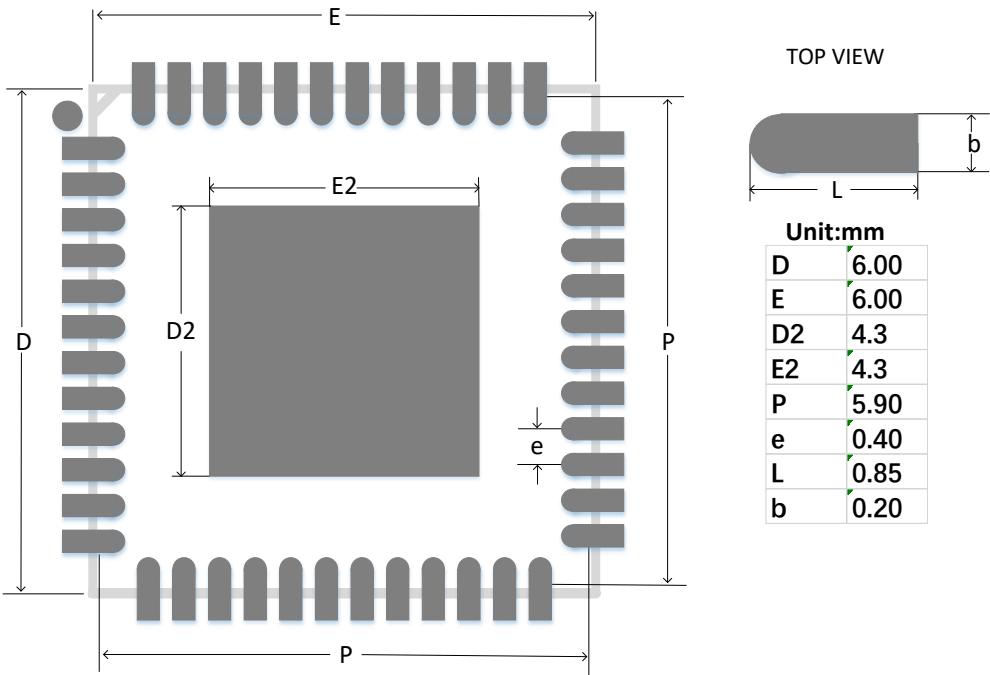


BOTTOM VIEW



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	—	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.40BSC		
Ne	4.40BSC		
Nd	4.40BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Figure 4-4 Recommended PCB Layout QN48



4.3 LQ100X Package Outline (14mm x 14mm, GW1AN-5)

Figure 4-5 Package Outline LQ100X

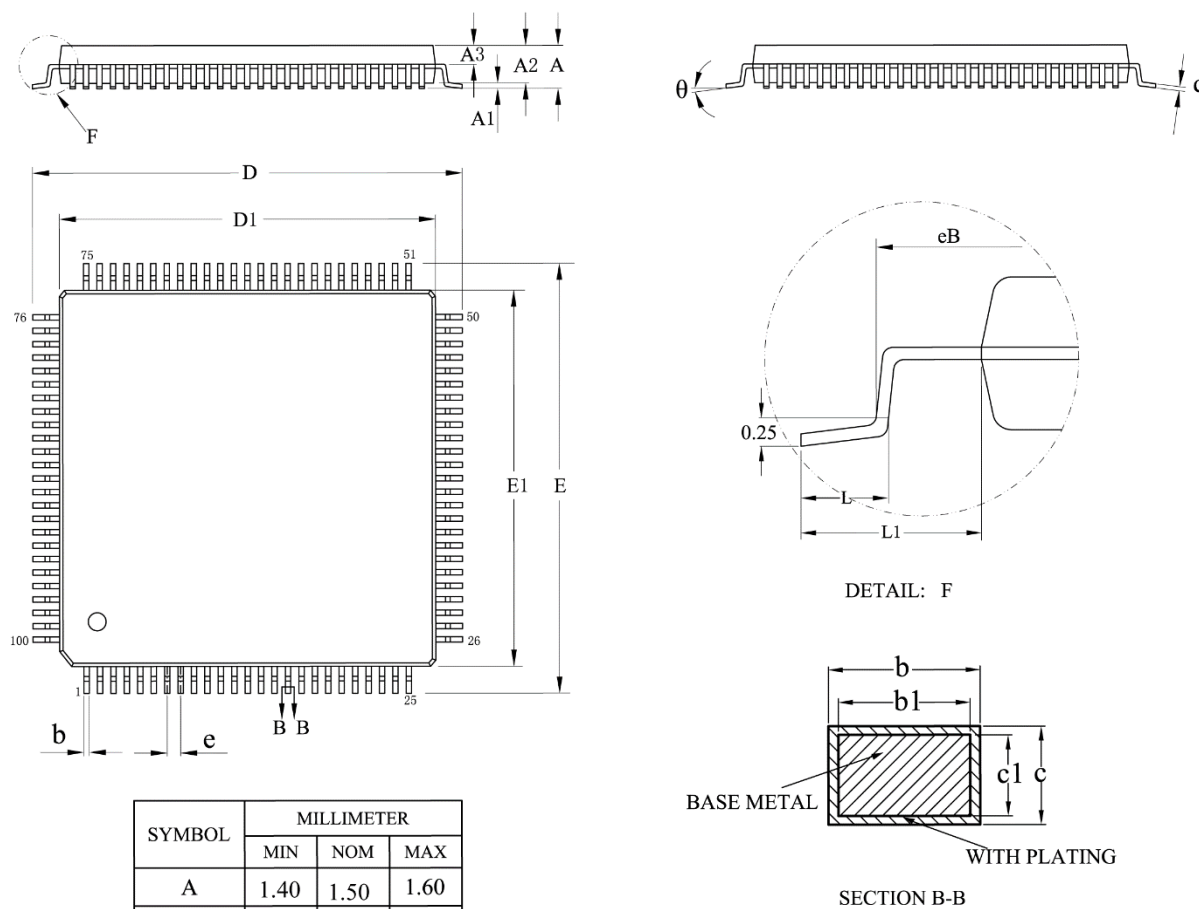
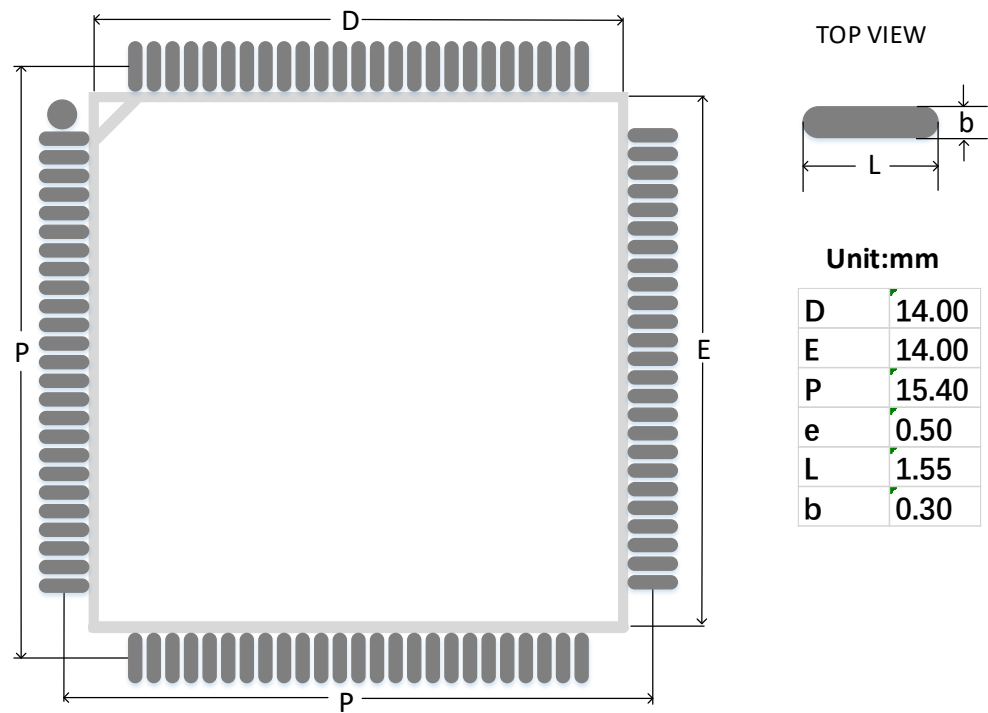
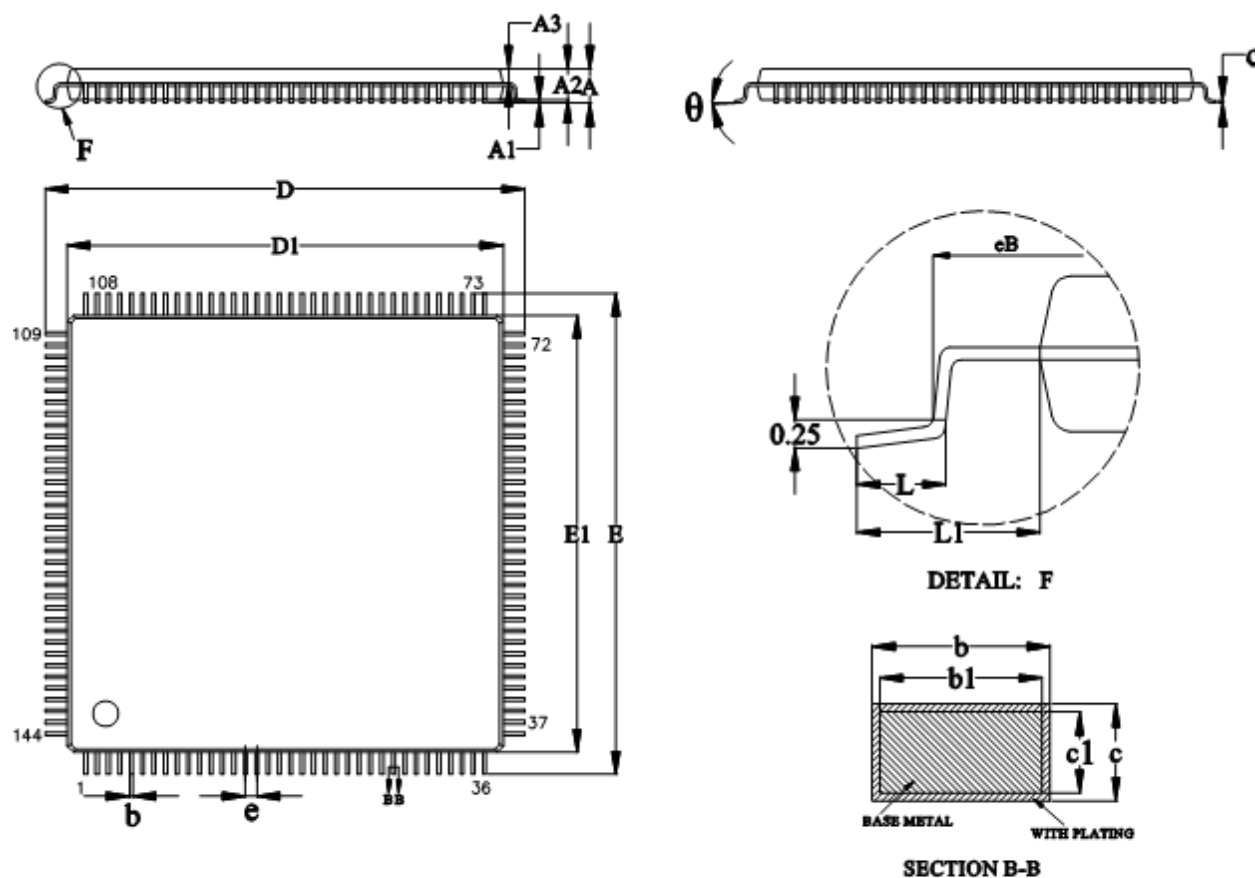


Figure 4-6 Recommended PCB Layout LQ100X



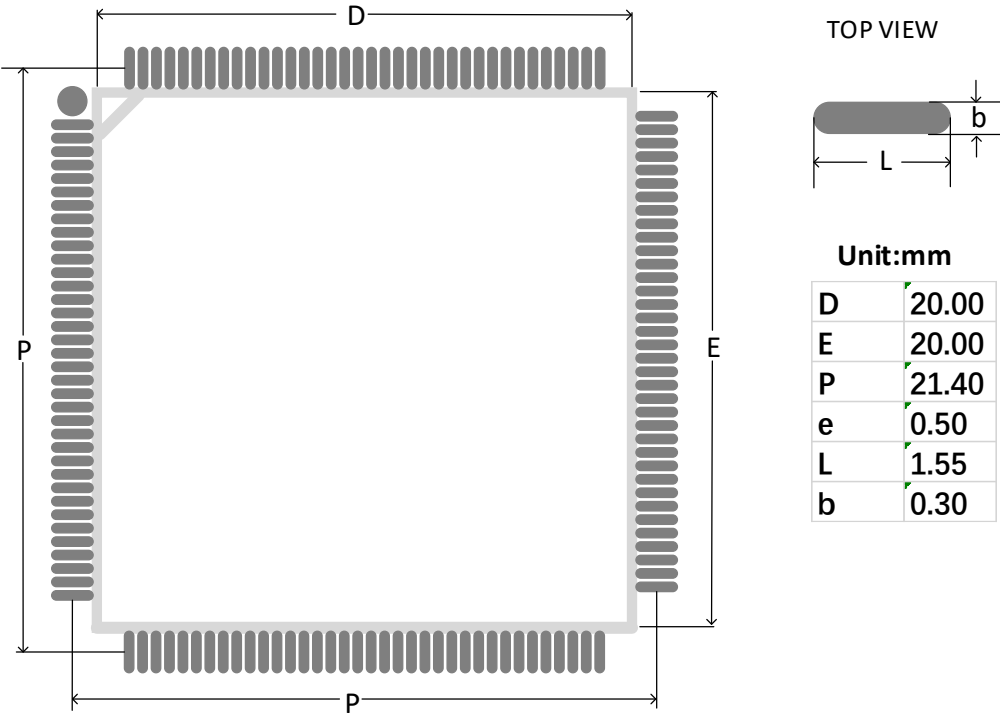
4.4 LQ144X Package Outline (20mm x 20mm, GW1AN-5)

Figure 4-7 Package Outline LQ144X



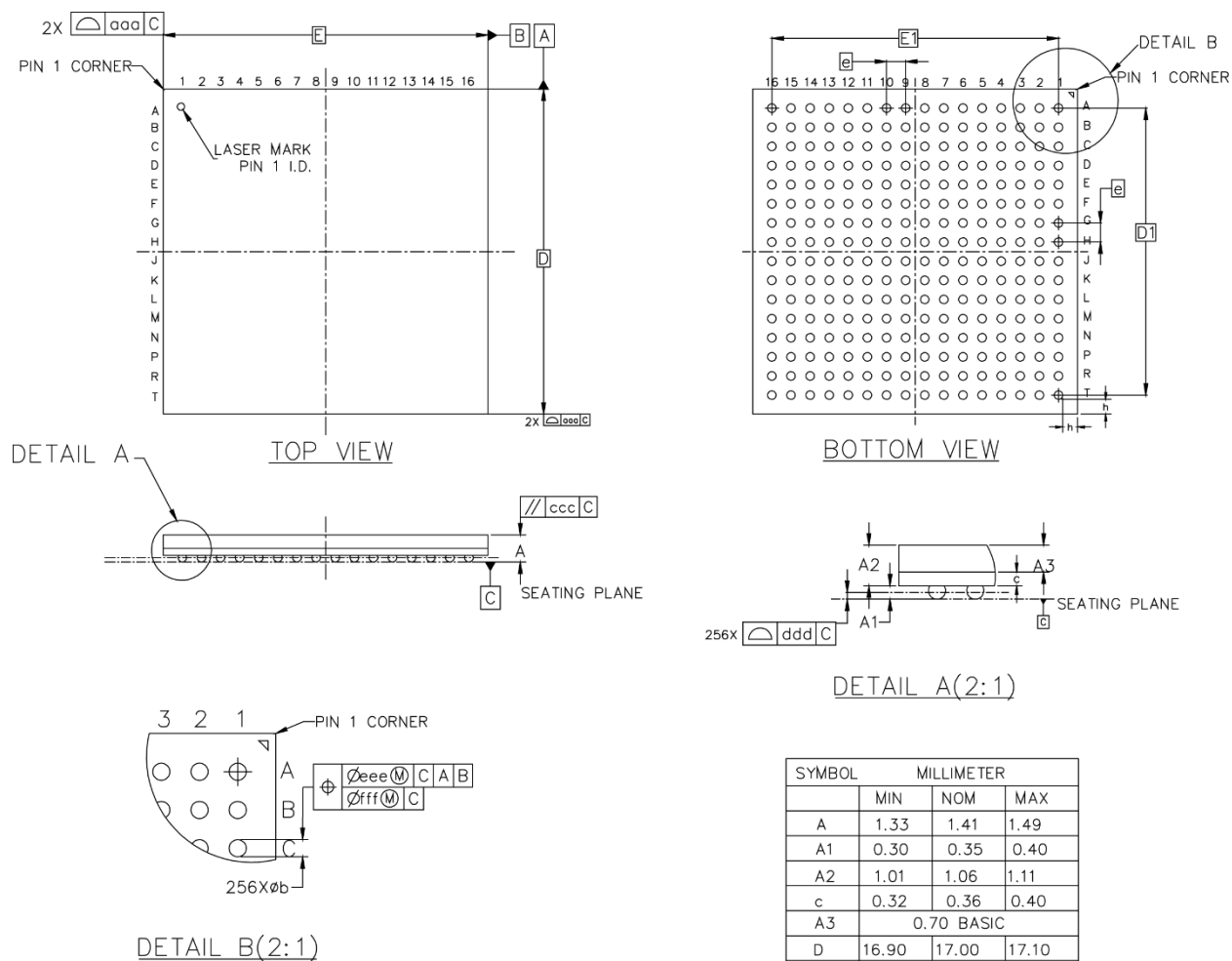
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

Figure 4-8 Recommended PCB Layout LQ144X



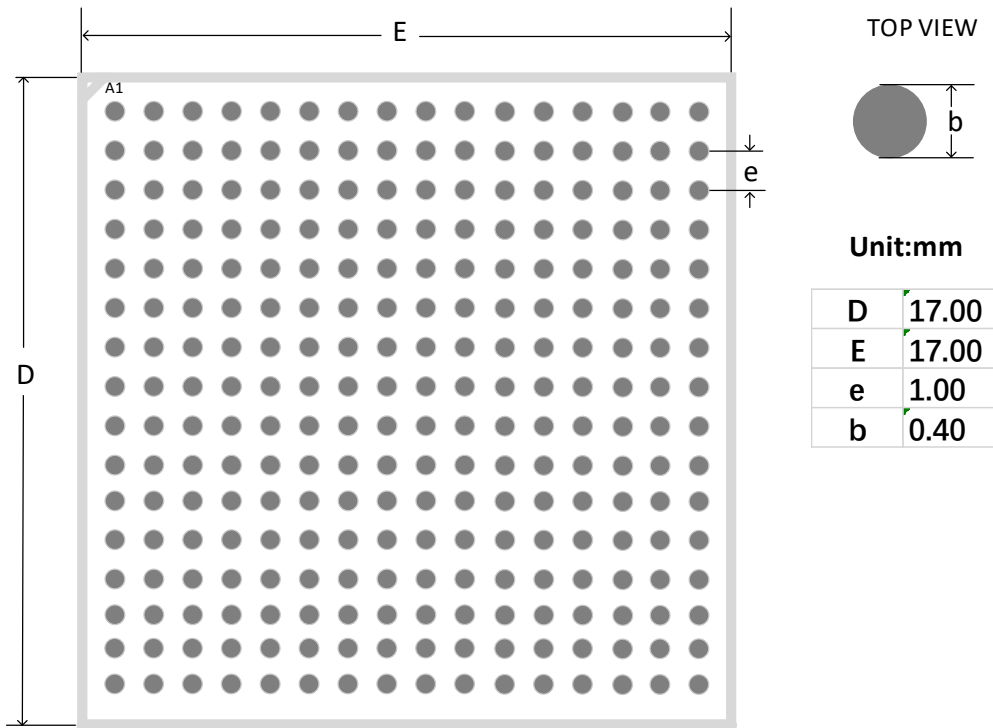
4.5 PG256X Package Outline (17mm x 17mm, GW1AN-5)

Figure 4-9 Package Outline PG256X



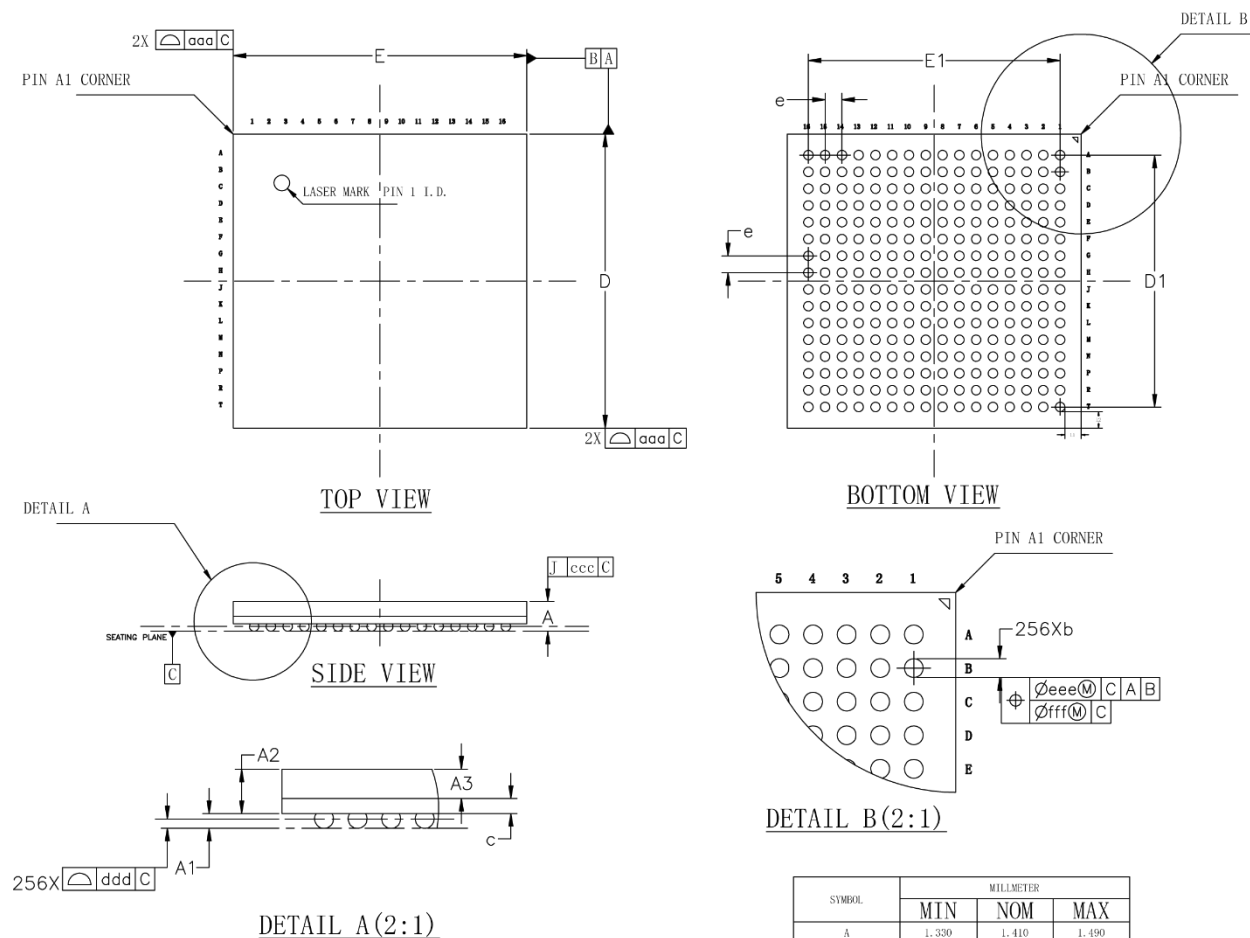
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.33	1.41	1.49
A1	0.30	0.35	0.40
A2	1.01	1.06	1.11
c	0.32	0.36	0.40
A3	0.70 BASIC		
D	16.90	17.00	17.10
D1	15.00 BASIC		
E	16.90	17.00	17.10
E1	15.00 BASIC		
e	1.00 BASIC		
b	0.40	0.45	0.50
h	0.700	0.775	0.850
aaa	0.15		
ccc	0.20		
ddd	0.20		
eee	0.15		
fff	0.08		

Figure 4-10 Recommended PCB Layout PG256X



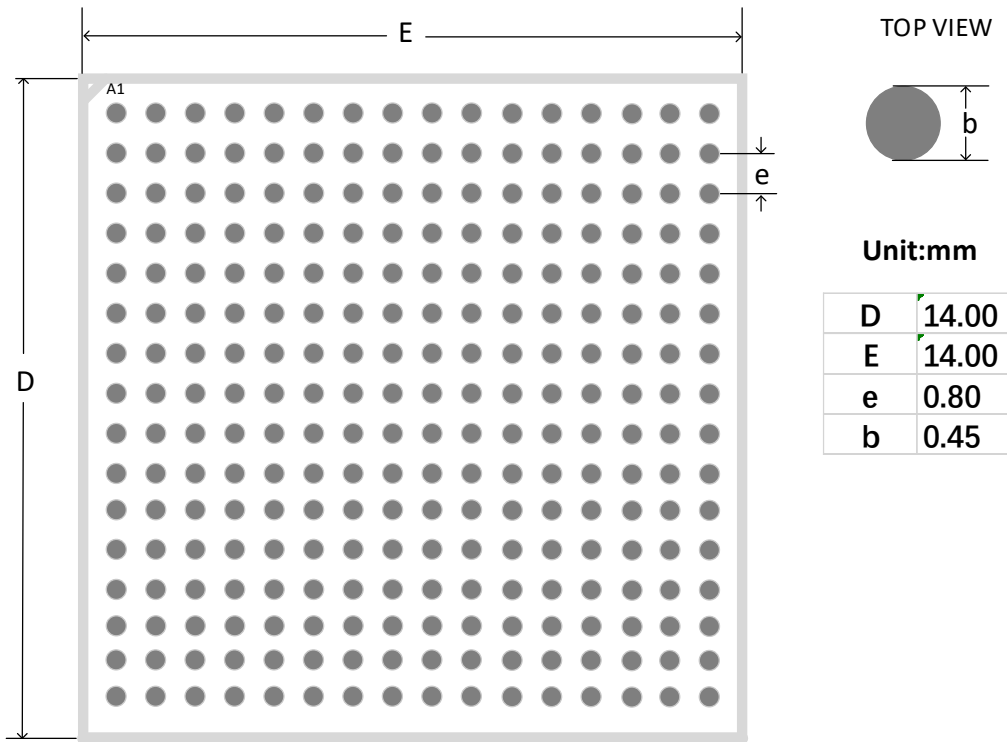
4.6 UG256X Package Outline (14mm x 14mm, GW1AN-5)

Figure 4-11 Package Outline UG256X



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.330	1.410	1.490
A1	0.300	0.350	0.400
A2	1.010	1.060	1.110
A3	0.700 BASIC		
C	0.320	0.360	0.400
D	13.900	14.000	14.100
D1	12.000 BASIC		
E	13.900	14.000	14.100
E1	12.000 BASIC		
e	0.800 BASIC		
b	0.400	0.450	0.500
L1	0.700	0.775	0.850
L2	0.700	0.775	0.850
aaa	0.150		
ccc	0.200		
ddd	0.200		
eee	0.150		
fff	0.080		

Figure 4-12 Recommended PCB Layout UG256X



Preliminary

