

FPGA CORE BOARD 4K/9K

Gowin FPGA 4K/9K LUTs, onboard high-GPIO expansion platform for industrial applications

GW1N-LV4-LQ100C6/I5 GW1N-LV9-LQ100C6/I5 USER GUIDE

13/11/2025

FPGA CORE BOARD 4K/9K

Gowin FPGA 4K/9K LUTs, onboard high-GPIO expansion platform for industrial applications

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Revision History

Date	Version	Description
13/11/2025	1.0	Initial version published

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1 About This Guide

1.1 Purpose

The GW1N-LV4(9)-LQ100C6/I5_V1.0 development board user manual consists of the following four parts:

- A brief introduction to the features and hardware resources of the development board
- An introduction to the hardware circuits functions, circuit, and pinout
- Considerations for the use of the development board
- Introduction to the use of the FPGA development software.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com

- <https://cdn.gowinsemi.com.cn/UG103E.pdf>
- <https://cdn.gowinsemi.com.cn/DS100E.pdf>
- <https://cdn.gowinsemi.com.cn/UG105E.pdf>
- <http://cdn.gowinsemi.com.cn/UG290E.pdf>
- <http://cdn.gowinsemi.com.cn/SUG100E.pdf>

1.3 Abbreviations and Terminology

Abbreviations and Terminology	Full Name
BSRAM	Block SRAM
DLL	Delay-locked Loop
DSP	Digital Signal Processing
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input Output
LDO	Low Dropout Regulator
LED	Light Emitting Diode
LQ100	LQFP100
LUT4	Four-input Look-up Table
PLL	Phase-locked Loop
SSRAM	Shadow SRAM

1.4 Support and Feedback

Onekiwi Technology provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

- Website: <https://onekiwi.com.vn/>
- Email: support@ontech.com.vn

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2 Development Board Description

2.1 Target FPGA device comparison

In this board we use two version Chip (They have the same Pinout):

- GW1N-LV4LQ100C6I5
- GW1N-LV9LQ100C6I5

Features	GW1N-4 LQFP100	GW1N-9 LQFP100
Logic Resources		
LUT4	4,608	8,640
Flip-Flops	3,456	6,480
Block Memory		
Block-SRAM	180 Kbit	468 Kbit
User Flash	256 Kbit	608 Kbit
DSP		
DSP 18×18	16	20
Clock Resources		
PLL	2	2
DLL	2	4
I/O (Package LQFP100)		
Max User I/O	79	79

2.2 Overview

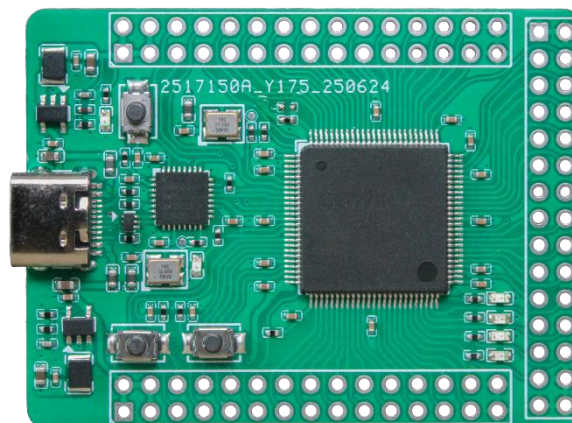


Figure 1 Front view of Development board

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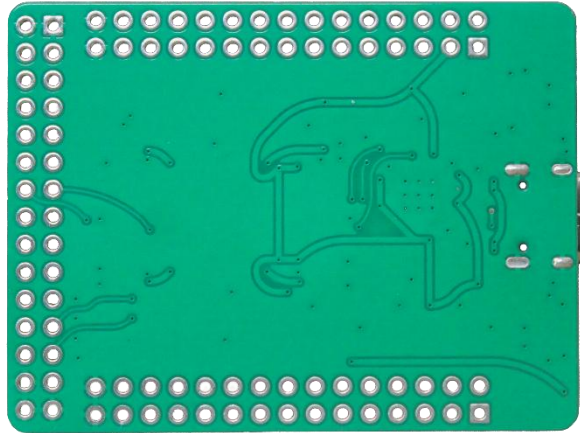


Figure 2 Back view of Development board

The Development board adopts the GW1N-LV4(9)LQ100C6I5 devices of the GW1N series of FPGA products. It features a range of advanced features including low power consumption, instant start-up, high security, low-cost, and flexible extensions, all of which can effectively reduce the learning cost and help users quickly design and develop programmable logic devices.

The development board includes 78 GPIOs ports. These provide users with a hardware evaluation and testing platform that offers a high integration level and stable performance VCCIO regulation (3.3 V). The development board also offers slide switches, key switches, a clock, and LEDs, all of which are useful for both developers and hobbyists alike.

With abundant GPIO resources, the development board can be used as the main board to design an image-sampling system and the other related systems by combining video daughter boards. Motion control systems can also be designed by combining the development board with AD/DA industrial daughter boards, while human-computer interface and image processing can be realized by combining the development board with the display daughter board.

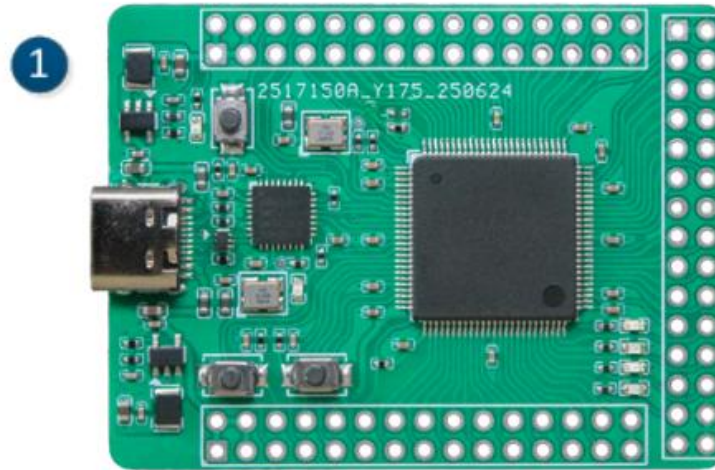
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2.3 A Development Board Suite

A development board suite includes the following items:

- Onekiwi_GW1N-LV4(9)LQ100C6I5_V1.0 development board
- USB type C



1. Development board



2. USB cable type C

Figure 3 A development board suite

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2.4 PCB components

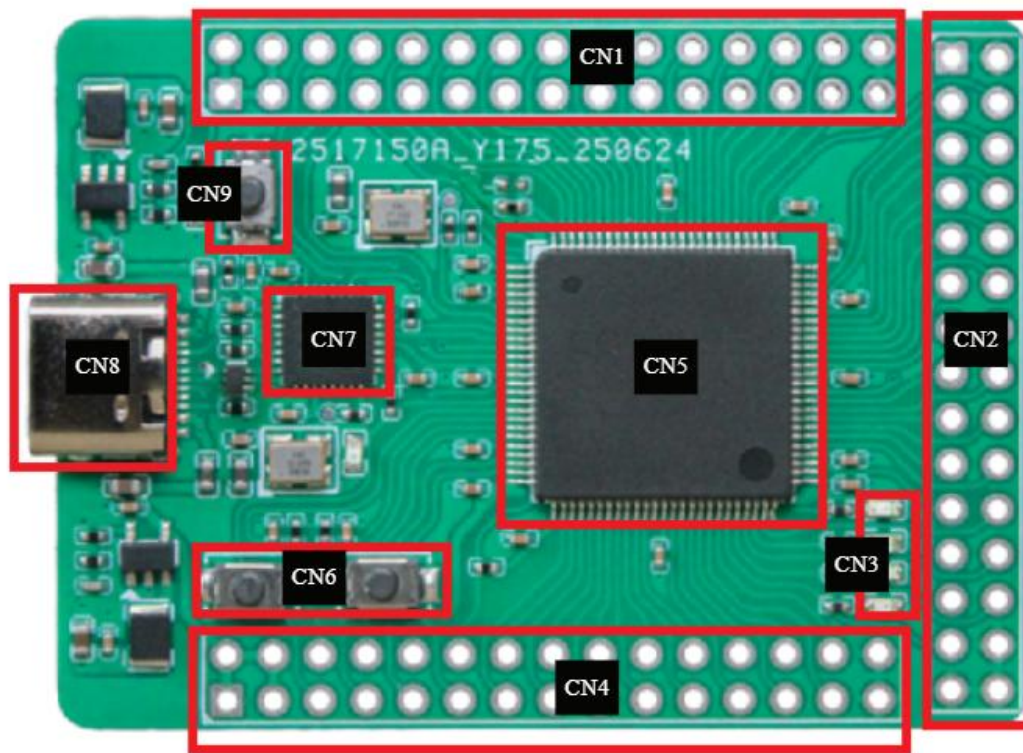


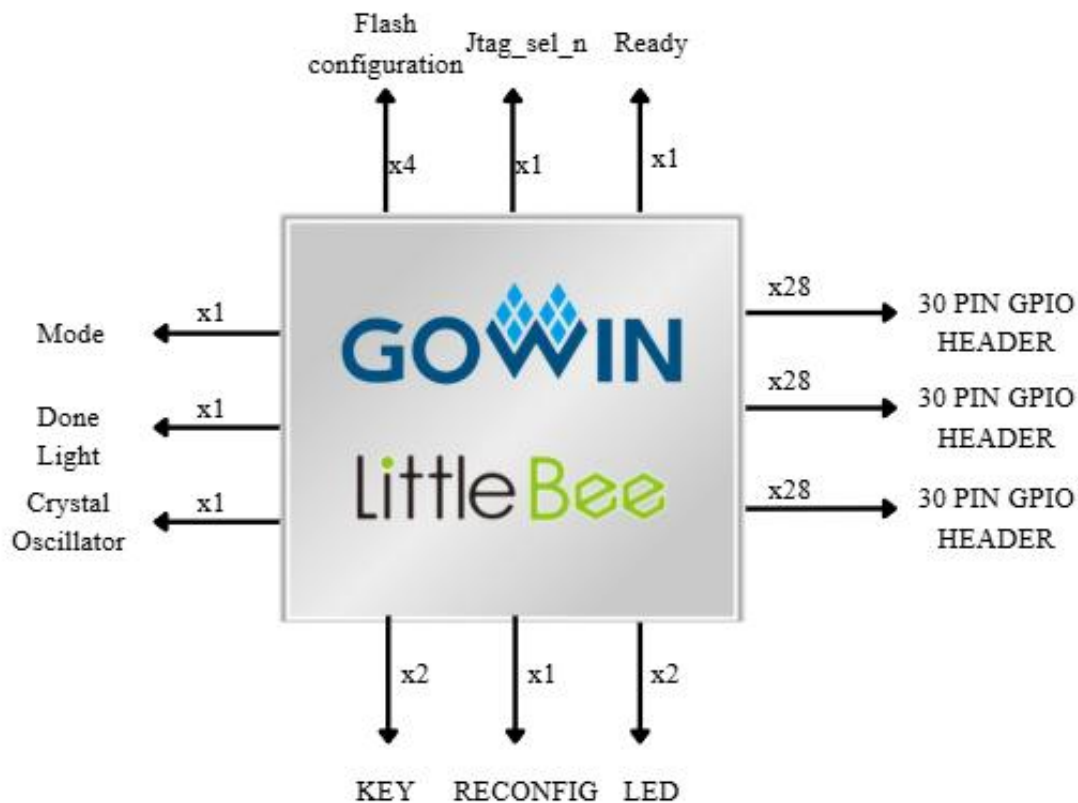
Figure 4 Board Components

CN	Name
CN1,CN2,CN4	GPIOs PIN
CN3	LED
CN5	FPGA Chip
CN6	Button
CN7	GWU2X for JTAG
CN8	USB-TYPEC
CN9	Reconfig button

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2.5 System Architecture



2.6 Features

- **FPGA CORE**
 - GW1N-LV4 Or GW1N-LV9 FPGA
 - Built-in Flash
 - LUT4 + BSRAM
 - GPIOs
- **POWER SYSTEM**
 - 5V Input
 - 3.3V (I/O, interface)
 - Protection: TVS, filters
- **CLOCK**
 - 27 MHz Oscillator → FPGA
 - 12 MHz Oscillator → USB GWU2X Interface

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- **USB INTERFACE**

- GWU2X chip
- USB-C Connector

- **GPIO HEADERS**

- 3 × 30-pin headers
- 70+ GPIOs

- **USER INPUT + OUTPUT**

- 3× Keys
 - 2x User
 - 1x Reconfigure
- Reset
- 6× LEDs
 - Power
 - DONE
 - 4× User

- **SPI FLASH**

- 64Mbit MSPI Flash for config

- **JTAG**

- TCK, TMS, TDI, TDO via header

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2.7 Development Board Specification

Table 1 Development Board specification

No.	Item	Functional Description	Technical Conditions	Note
1	FPGA	Core chip GW1N-LV4(9) LQ100C6I5	—	—
2	Download Interface	Support USB interface; Support JTAG, AUTOBOOT, MSPI	USB-JTAG module on board (GWU2X)	—
3	Power Supply	Provide USB Type C 5V input	Input power: 5V Provide power for FPGA, USB-JTAG circuit and peripherals via 5V→3.3V circuit•	—
5	Key Switches	Available for testing	2	—
6	Reset Button	Reset for FPGA	1	—
7	LED	Test indicator, DONE indicator, Power indicator	• Four test indicators (green) • One DONE indicator (green) • One Power indicator (green)	—
8	Crystal Oscillator	Provide system clock for FPGA	• 27 MHz crystal oscillator (FPGA clock) • 12 MHz crystal oscillator (USB interface)	—
10	GPIO	I/O interface for user extension and testing	• 3 × 30-pin GPIO headers • Approximately 70+ GPIO pins available • Supports 3.3V I/O voltage (per FPGA bank)	—
12	Protection	• USB interface: ESD protection• Power interface: reverse-current and over-current protection	• USB ESD protection: ±15 kV air discharge, ±8 kV contact discharge • Schottky diode for reverse-current protection • 2A self-recovery fuses at power input	—
13	Voltage	—	Input range: 5V USB-C	—
14	Humidity	—	95%	—
15	Temperature	—	Operating range: -20°C ~ 70°C	—

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3 FPGA Circuits

3.1 FPGA Module

Overview

For the resources of GW1N series of FPGA Products, refer to <http://cdn.gowinsemi.com.cn/DS100E.pdf>

I/O Bank Introduction

For the I/O BANK, package, and pinout information, see <https://cdn.gowinsemi.com.cn/UG103E.pdf> for more details.

3.2 Download Interface

3.2.1 Overview

The development board provides an USB download interface. The data stream file can be downloaded to the internal SRAM, internal flash, or external flash as needed.

Note!

- When downloaded to SRAM, the data stream file will be lost if the device is power down, and it will need to be downloaded again after power-on.
- If downloaded to flash, the data stream file will not be lost if the device is powered down.

3.2.2 USB Download Circuit

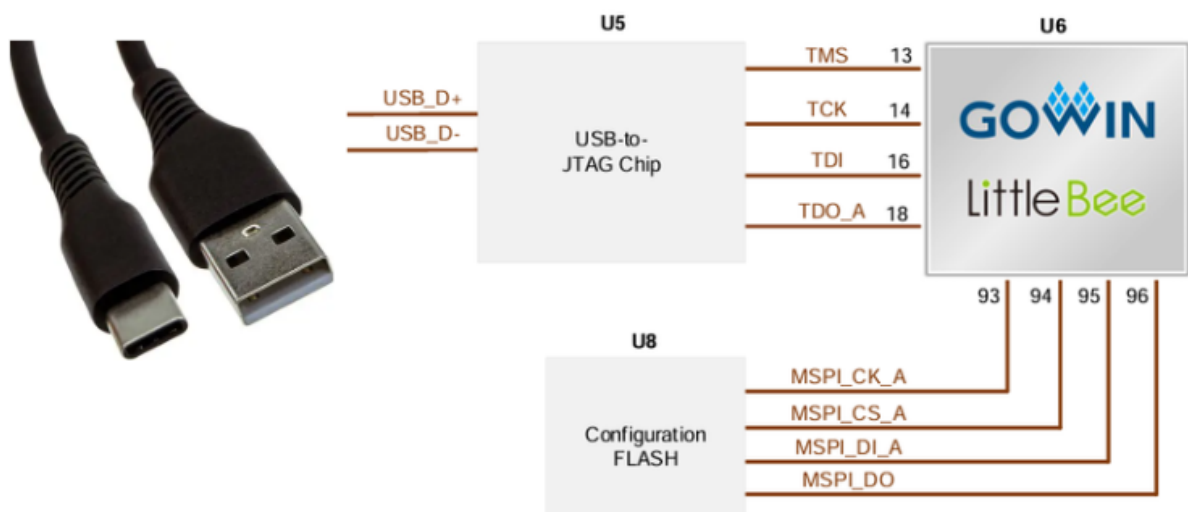


Figure 5 Connection Diagram for FPGA USB Downloading and Configuration

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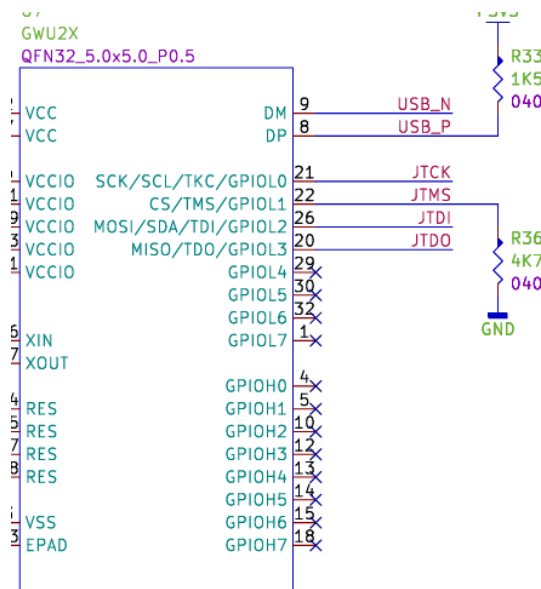


Figure 6 GWU2X USB to JTAG chip

3.2.3 Downloading the Data Stream

The data stream file can be downloaded in the following ways.

1. SRAM

Scan the device and download the bit file after powering the device on. The Done indicator lights up to denote that the download has been successful.

2. Internal Flash

Power on and download. After downloading the data stream file successfully, power down to reset and load the bit file from the internal Flash, and when the Done indicator lights up to denote that the download has been successful.

3. External Flash Configuration

Power on and download. Power down to reset and load the bit file from the external flash. The Done indicator lights up to denote that the download has been successful.

3.2.4 Pinout

Table 2 Download Pinout

Signal Name	Pin No.	BANK	Description	I/O
JTMS	8	3	JTAG Signal	VCCIO3
JTCK	9	3	JTAG Signal	VCCIO3
JTDI	11	3	JTAG Signal	VCCIO3
JTDO	12	3	JTAG Signal	VCCIO3
MSPI_CK	65	1	FLASH signals configuration	VCCIO1
MSPI_CS	66	1	FLASH signals configuration	VCCIO1
MSPI_MI	68	1	FLASH signals configuration	VCCIO1
MSPI_MO	67	1	FLASH signals configuration	VCCIO1

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3.3 Power Supply

3.3.1 Overview

The 5V input power interface has overcurrent and inverse current protection. The overcurrent limit is 2A.

The TI LDO power supply chip is used to step down voltage from 5V to 3.3V. The power supply can support up to 2A, which can meet the power demand of the development board.

3.3.2 Power System Distribution

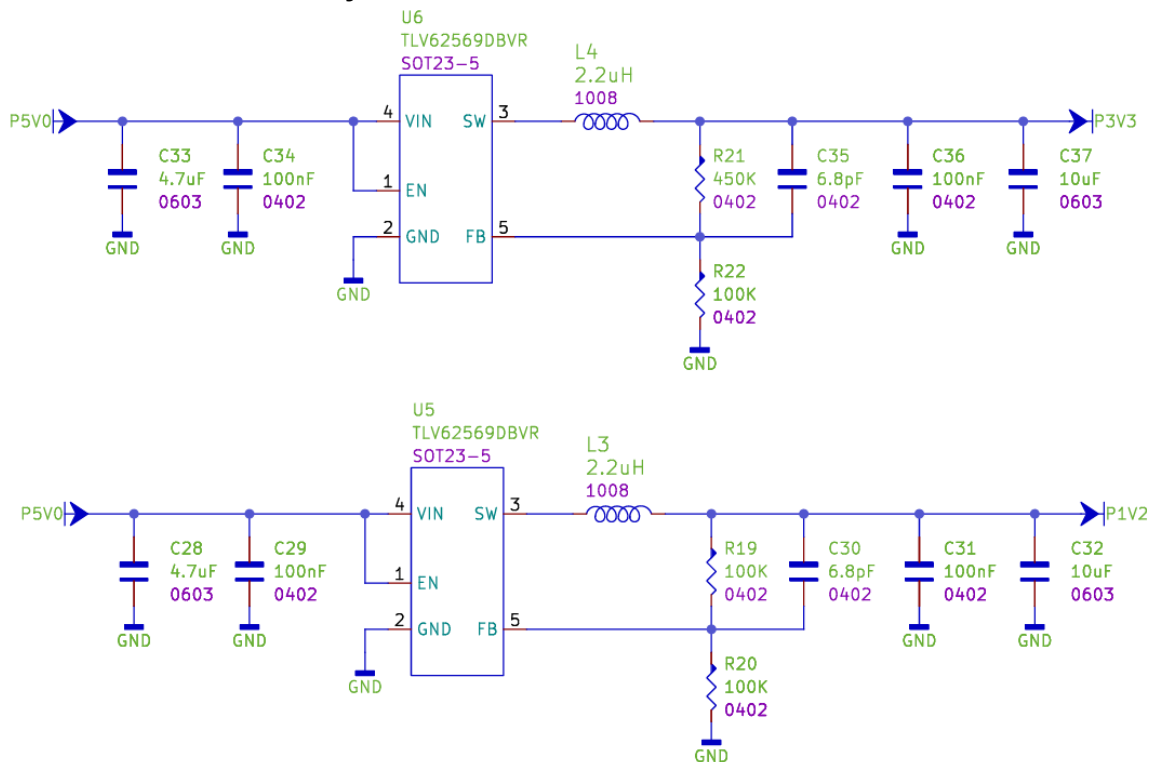


Figure 7 Power distribution

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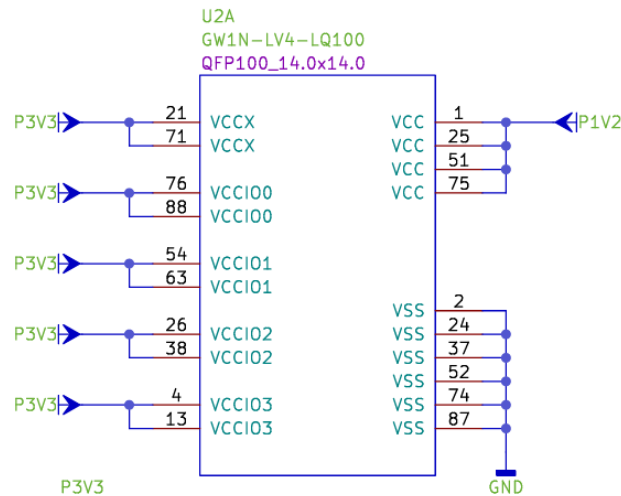


Figure 8 Power banks

3.3.3 Power Pinout

ALL I/O Banks are 3V3.

3.4 Clock, Reset

3.4.1 Overview

A 27MHz crystal oscillator is provided in the development board that connects to the PLL input pin. This can be employed as the input clock for the PLL in FPGA, and the output clock as needed via multiplication and division of the PLL frequency.

To facilitate testing, a SMA socket is reserved on the development board as the clock input interface. The clock signal is connected to the FPGA global clock pin.

3.4.2 Clock, Reset

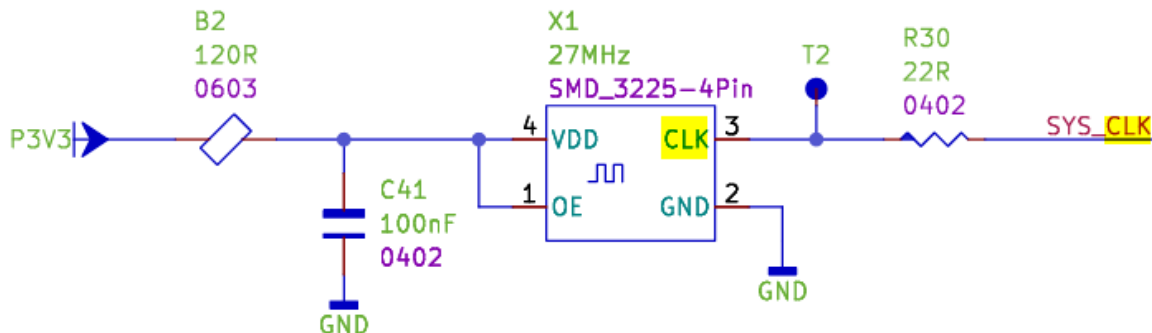


Figure 9 Clock

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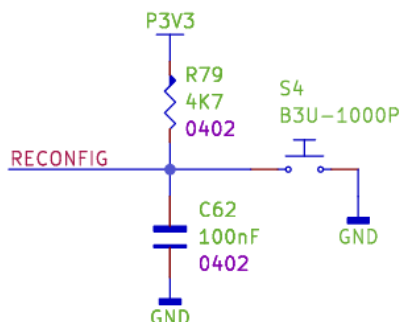


Figure 10 Reset

3.4.3 Pinout

Signal Name	Pin No.	BANK	Description	I/O
SYS_CLK	6	3	27 MHz crystal oscillator input	3.3V
RECONFIG	14	3	Reset signal	3.3V

Table 3 Clock,reset Pinout

3.5 LED

3.5.1 Overview

Four green LEDs are incorporated into the development board and are used to display the required status. In addition, two LEDs are reserved to signify power supply and FPGA loading status.

Users can test the LEDs in the following ways:

- If the output signal of related pins is logic low, LED is on.
- If logic is high, LED is off.

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3.5.2 LED Circuit

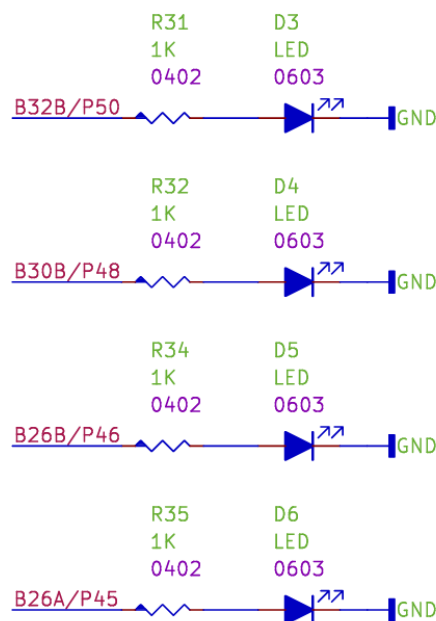


Figure 11 Led circuit

3.5.3 Pinout

Table 4 Led pinout

Signal Name	Pin No.	BANK	Description	I/O
B32B	50	2	LED1	3.3V
B30B	48	2	LED2	3.3V
B26B	46	2	LED3	3.3V
B26A	45	2	LED4	3.3V

3.6 Key

3.6.1 Overview

Two key switches are embedded in the development board. Users can manually input a low level to the corresponding FPGA pins for testing purposes.

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3.6.2 Key Circuit

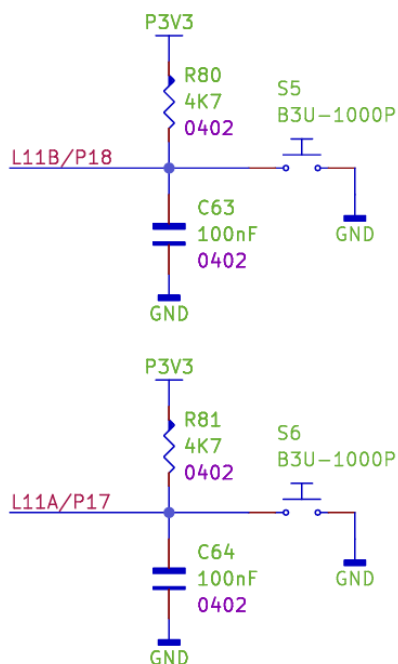


Figure 12 Key circuit

3.6.3 Pinout

Table 5 Key pinout

Signal Name	Pin No.	BANK	Description	I/O
L11B	18	2	KEY1	3.3V
L11A	17	2	KEY2	3.3V

3.7 GPIO

3.7.1 Overview

Three 2.54mm DC3-30P sockets are reserved on the development board for user function extension and testing purposes.

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3.7.2 GPIO Circuit

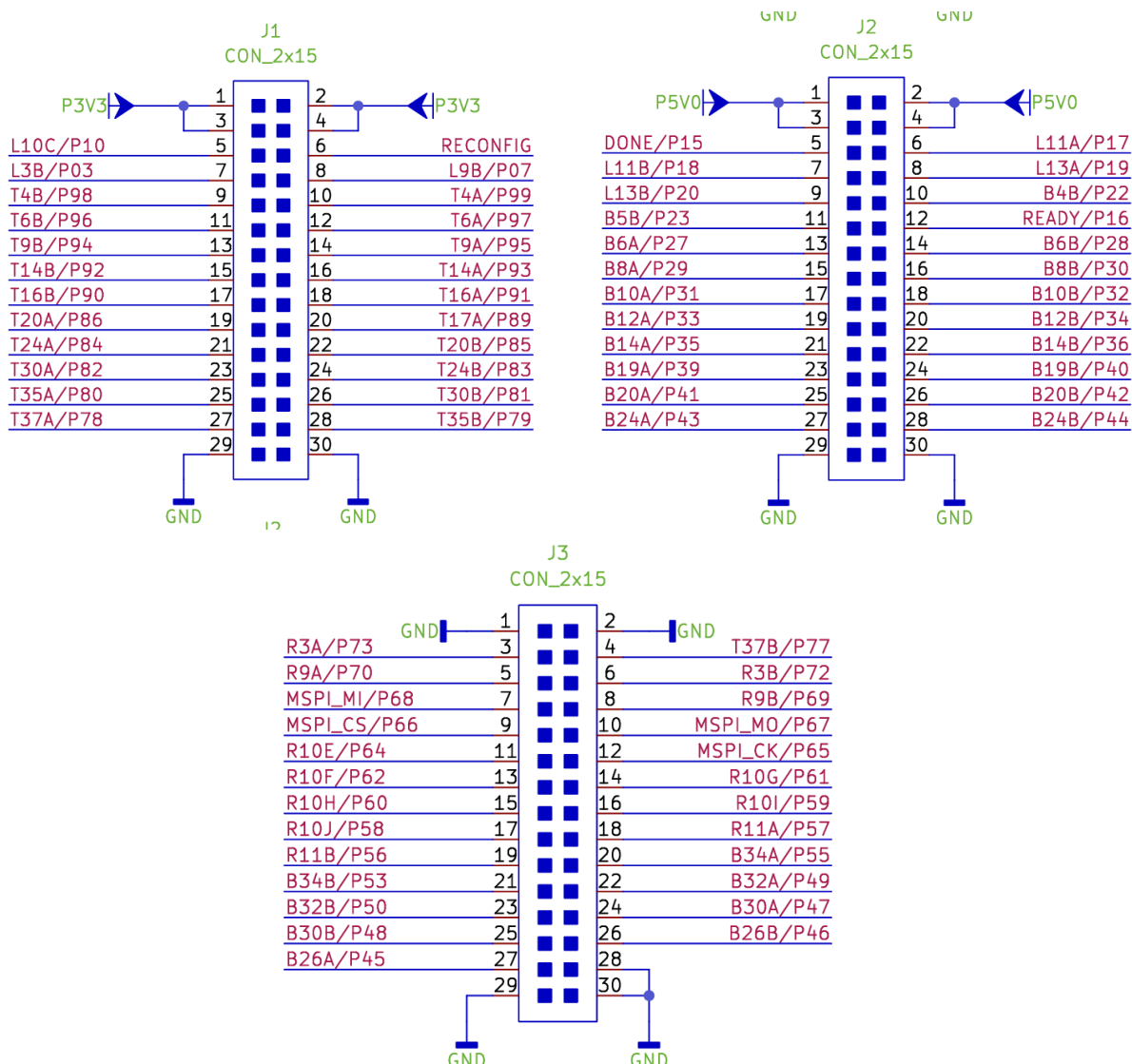


Figure 3 GPIO circuits

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3.7.3 Pinout

Table 6 J1 Pinout

Signal Name	Pin No.	30P Socket Pin No.	BANK	Description	I/O
P3V3	—	1	—	Power	3.3V
P3V3	—	2	—	Power	3.3V
P3V3	—	3	—	Power	3.3V
P3V3	—	4	—	Power	3.3V
L10C	10	5	3	General I/O	3.3V
RECONFIG	14	6	3	Reconfig Input	3.3V
L3B	3	7	3	General I/O	3.3V
L9B	7	8	3	General I/O	3.3V
T4B	98	9	0	General I/O	3.3V
T4A	99	10	3	General I/O	3.3V
T6B	96	11	0	General I/O	3.3V
T6A	97	12	3	General I/O	3.3V
T9B	94	13	0	General I/O	3.3V
T9A	95	14	3	General I/O	3.3V
T14B	92	15	0	General I/O	3.3V
T14A	93	16	3	General I/O	3.3V
T16B	90	17	0	General I/O	3.3V
T16A	91	18	3	General I/O	3.3V
T20A	86	19	0	General I/O	3.3V
T17A	89	20	3	General I/O	3.3V
T24A	84	21	0	General I/O	3.3V
T20B	85	22	3	General I/O	3.3V
T30A	82	23	0	General I/O	3.3V
T24B	83	24	0	General I/O	3.3V
T35A	80	25	0	General I/O	3.3V
T30B	81	26	0	General I/O	3.3V
T37A	78	27	0	General I/O	3.3V
T35B	79	28	0	General I/O	3.3V
GND	—	29	—	Ground	—
GND	—	30	—	Ground	—

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Table 7 J2 Pinout

Signal Name	Pin No.	30P Socket Pin No.	BANK	Description	I/O
P5V0	—	1	—	Power	5V
P5V0	—	2	—	Power	5V
P5V0	—	3	—	Power	5V
P5V0	—	4	—	Power	5V
DONE	15	5	3	DONE indicator / status	3.3V
L11A	17	6	3	General I/O	3.3V
L11B	18	7	3	General I/O	3.3V
L13A	19	8	3	General I/O	3.3V
L13B	20	9	3	General I/O	3.3V
B4B	22	10	3	General I/O	3.3V
B5B	23	11	3	General I/O	3.3V
READY	16	16	3	READY / status	3.3V
B6A	27	13	2	General I/O	3.3V
B6B	28	14	2	General I/O	3.3V
B8A	29	15	2	General I/O	3.3V
B8B	30	16	2	General I/O	3.3V
B10A	31	17	2	General I/O	3.3V
B10B	32	18	2	General I/O	3.3V
B12A	33	19	2	General I/O	3.3V
B12B	34	20	2	General I/O	3.3V
B14A	35	21	2	General I/O	3.3V
B14B	36	22	2	General I/O	3.3V
B19A	39	23	2	General I/O	3.3V
B19B	40	24	2	General I/O	3.3V
B20A	41	25	2	General I/O	3.3V
B20B	42	26	2	General I/O	3.3V
B24A	43	27	2	General I/O	3.3V
B24B	44	28	2	General I/O	3.3V
GND	—	29	—	Ground	—
GND	—	30	—	Ground	—

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Table 8 J3 Pinout

Signal Name	Pin No.	30P Socket Pin No.	BANK	Description	I/O
GND	—	1	—	Ground	—
GND	—	2	—	Ground	—
R3A	73	3	1	General I/O	3.3V
T37B	77	4	0	General I/O	3.3V
R9A	70	5	1	General I/O	3.3V
R3B	72	6	1	General I/O	3.3V
MSPI_MI	68	7	1	MSPI / Flash MI	3.3V
R9B	69	8	1	General I/O	3.3V
MSPI_CS	66	9	1	MSPI Chip Select	3.3V
MSPI_MO	67	10	1	MSPI / Flash MO	3.3V
R10E	64	11	1	General I/O	3.3V
MSPI_CK	65	12	1	MSPI Clock	3.3V
R10F	62	13	1	General I/O	3.3V
R10G	61	14	1	General I/O	3.3V
R10H	60	15	1	General I/O	3.3V
R10I	59	16	1	General I/O	3.3V
R10J	58	17	1	General I/O	3.3V
R11A	57	18	1	General I/O	3.3V
R11B	56	19	1	General I/O	3.3V
B34A	55	20	2	General I/O	3.3V
B34B	53	21	2	General I/O	3.3V
B32A	49	22	2	General I/O	3.3V
B32B	50	23	2	General I/O	3.3V
B30A	47	24	2	General I/O	3.3V
B30B	48	25	2	General I/O	3.3V
B26B	46	26	2	General I/O	3.3V
B26A	45	27	2	General I/O	3.3V
Spare / NC	—	28	—	Spare / NC	—
GND	—	29	—	Ground	—
GND	—	30	—	Ground	—

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4 Consideration

Considerations for the use of the development board:

1. Handle with care and pay attention to electrostatic protection.
2. When downloading bitstream files to internal flash or external flash, set the MODE pin state to the correct configuration value, please refer to: <https://cdn.gowinsemi.com.cn/UG290E.pdf>
3. Power input 5V