

Evaluation Kit Onekiwi FPGA 1P5 USER GUIDE

5/12/2025

EVK For Kiwi FPGA 1P5

Gowin FPGA 1P5

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EVK For Kiwi FPGA 1P5

Gowin FPGA 1P5

Revision History

Date	Version	Description
5/7/2025	1.0	First prototype
5/12/2025	2.0	Initial version published

EVK For Kiwi FPGA 1P5

Gowin FPGA 1P5

Contents

1	About This Guide.....	6
1.1	Purpose	6
1.2	Related Documents.....	6
1.3	Abbreviations and Terminology	6
1.4	Support and Feedback.....	6
2	Development Board Description.....	7
2.1	Overview.....	7
2.2	A Development Board Suite	8
2.3	PCB components	9
2.4	System Architecture.....	9
3	FPGA Circuits.....	11
3.1	FPGA Module.....	11
3.2	Connect Kiwi 1P5 and EVK.....	11
3.2.1	Pin header for GPIOs Kiwi 1P5	11
3.2.2	How to connect.....	11
3.3	Power Supply(Kiwi 1P5 board).....	12
3.3.1	Overview	12
3.3.2	Power System Distribution	13
3.4	Clock(Kiwi 1P5 board).....	13
3.4.1	Overview	13
3.4.2	Clock.....	13
3.4.3	Pinout.....	13
3.5	LED (kiwi 1P5 board)	14
3.5.1	Overview	14
3.5.2	LED Circuit.....	14
3.5.3	Pinout.....	14
3.6	Key(kiwi 1P5 board).....	14
3.6.1	Overview	14
3.6.2	Key Circuit	15
3.6.3	Pinout.....	15
3.7	Key(EVK).....	16
3.7.1	Key circuit	16
3.7.2	Pinout.....	16
3.8	LED 7 segments.....	16
3.8.1	LED 7 Segments Circuit	16
3.8.2	Pinout.....	17
3.9	EEPROM IIC	17
3.9.1	EEPROM circuit.....	17
3.9.2	Pinout.....	17
3.10	RGB Led.....	18
3.10.1	RGB Circuit.....	18
3.10.2	Pinout.....	18
3.11	BUZZER.....	18
3.11.1	Buzzer Circuit	18
3.11.2	Pinout.....	18
3.12	OLED IIC	19
3.12.1	OLED circuit.....	19
3.12.2	Pinout.....	19
3.13	Grove	19

EVK For Kiwi FPGA 1P5

Gowin FPGA 1P5

3.13.1	Grove circuit.....	19
3.13.2	Pinout.....	19
3.14	Arduino Pin header.....	20
3.14.1	Arduino Pin header circuit	20
3.14.2	Pinout.....	20
3.15	Pin headers.....	21
3.15.1	Gpio circuits	21
3.15.2	Pinout.....	21
4	Consideration	22

Table of Figure

FIGURE 2-1	FRONT VIEW OF DEVELOPMENT BOARD	7
FIGURE 2-2	BACK VIEW OF DEVELOPMENT BOARD	7
FIGURE 2-3	DEVELOPMENT BOARD SUITE	8
FIGURE 2-4	ONEKIWI 1P5 EVK COMPONENTS	9
FIGURE 2-5	SYSTEM ARCHITECTURE	10
FIGURE 3-1	PIN HEADER FOR GPIOs KIWI 1P5	11
FIGURE 3-2	EVK RIGHT CONNECT WITH KIWI 1P5 BOARD	12
FIGURE 3-3	POWER DISTRIBUTION	13
FIGURE 3-4	CLOCK CIRCUIT	13
FIGURE 3-5	LED CIRCUIT	14
FIGURE 3-6	KEY CIRCUIT	15
FIGURE 3-7	KEY CIRCUIT	16
FIGURE 3-8	LED 7 SEGMENTS CIRCUIT	16
FIGURE 3-9	EEPROM CIRCUIT	17
FIGURE 3-10	RGB CIRCUIT	18
FIGURE 3-11	BUZZER CIRCUIT	18
FIGURE 3-12	OLED CIRCUIT	19
FIGURE 3-13	GROVE CIRCUIT	19
FIGURE 3-14	GROVE CIRCUIT	20
FIGURE 3-15	GROVE PINOUT.....	20
FIGURE 3-16	GPIO CIRCUIT	21
FIGURE 3-17	GPIO PINOUT	21

Table of Table

TABLE 1	TABLE OF ABBREVIATIONS AND TERMINOLOGY	6
TABLE 2	EVK COMPONENTS	9
TABLE 3	PINOUT CLOCK.....	13
TABLE 4	LED PINOUT	14
TABLE 5	KEY PINOUT	15
TABLE 6	KEY PINOUT	16
TABLE 7	LED 7 SEGMENTS PINOUT	17
TABLE 8	EEPROM CIRCUIT	17
TABLE 9	RGB PINOUT	18
TABLE 10	BUZZER PINOUT.....	19
TABLE 11	OLED PINOUT.....	19
TABLE 12	GROVE TABLE	20

1 About This Guide

1.1 Purpose

The EVK Kiwi 1P5 V2.0 development board user manual consists of the following four parts:

- A brief introduction to the features and hardware resources of the development board
- An introduction to the hardware circuits functions, circuit, and pinout
- Considerations for the use of the development board
- Introduction to the use of the FPGA development software.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com

- https://www.gowinsemi.com/upload/database_doc/3224/document/68d5f9f48daf0.pdf, datasheet
- https://www.gowinsemi.com/upload/database_doc/1766/document/6738b743e36fe.pdf, Pinout
- https://www.gowinsemi.com/upload/database_doc/3225/document/686f5c000196d.pdf, Schematic
- <https://cdn.gowinsemi.com.cn/UG290E.pdf> ,Gowin Programming and Configuration Guide
- <https://cdn.gowinsemi.com.cn/SUG100E.pdf> , Gowin software user guide

1.3 Abbreviations and Terminology

Abbreviations and Terminology	Full Name
BSRAM	Block SRAM
DLL	Delay-locked Loop
DSP	Digital Signal Processing
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input Output
LDO	Low Dropout Regulator
LED	Light Emitting Diode
LQ100	LQFP100
LUT4	Four-input Look-up Table
PLL	Phase-locked Loop
SSRAM	Shadow SRAM

Table 1 Table Of abbreviations and terminology

1.4 Support and Feedback

Onekiwi Technology provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

- Website: <https://onekiwi.com.vn/>

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Gowin FPGA 1P5

- Email: support@ontech.com.vn

2 Development Board Description

2.1 Overview



Figure 2-1 Front view of Development board

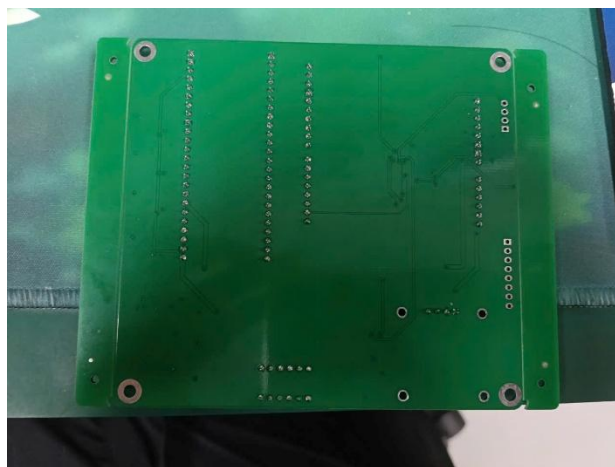


Figure 2-2 Back view of Development board

Unlock the full potential of programmable logic with the OneKiwi 1P5 Evaluation Kit. This all-in-one platform transforms the compact OneKiwi 1P5 FPGA module into a fully-featured development station. Designed with education and rapid prototyping in mind, the carrier board hosts a suite of essential components essential for mastering digital logic design.

From driving complex displays like the OLED and 7-segment LEDs to managing communication protocols with the on-board EEPROM, this EVK covers it all. Users can easily experiment with state machines using the push buttons and buzzer, or dive into timing protocols with the WS2812 RGB LEDs. Additionally, the inclusion of Arduino-style GPIO headers ensures that your project can grow beyond the board, offering limitless possibilities for connectivity and expansion.

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2.2 A Development Board Suite

A development board suite includes the following items:

- EVK for 1P5 board
- USB type C
- EVK for 1P5 board

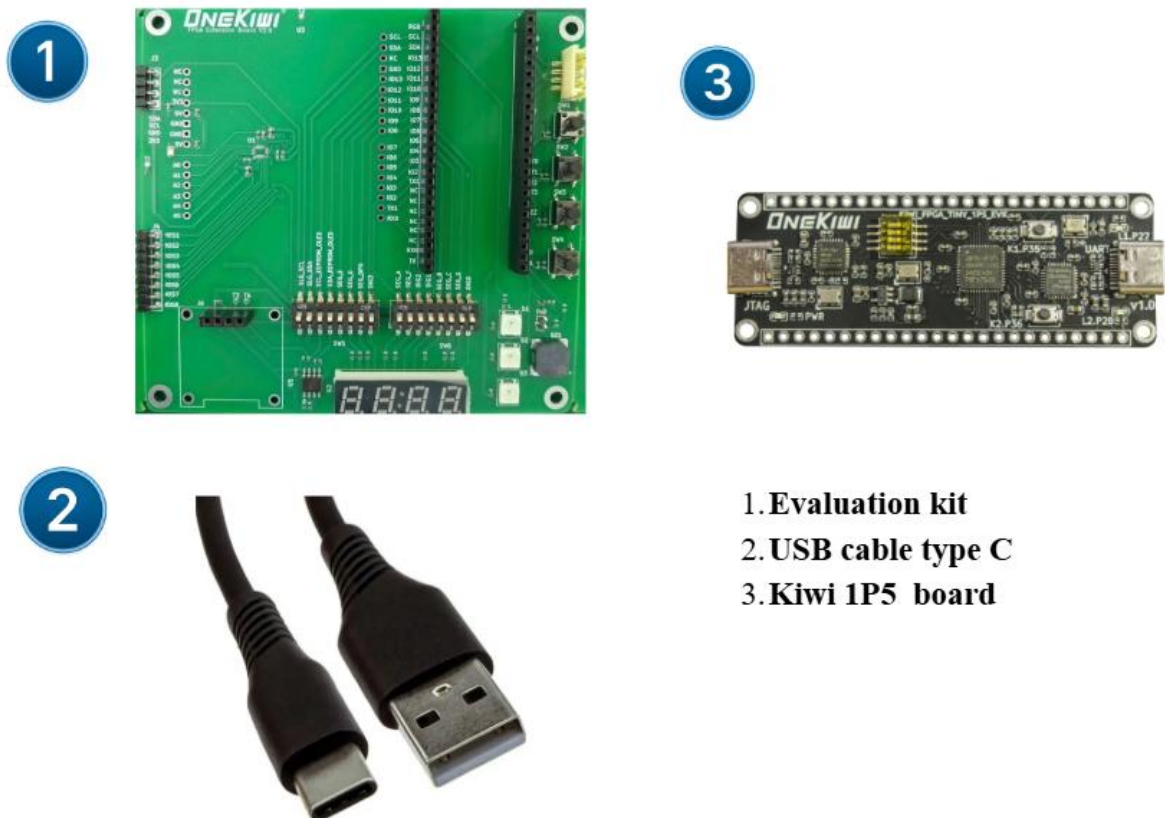


Figure 2-3 Development board suite

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2.3 PCB components

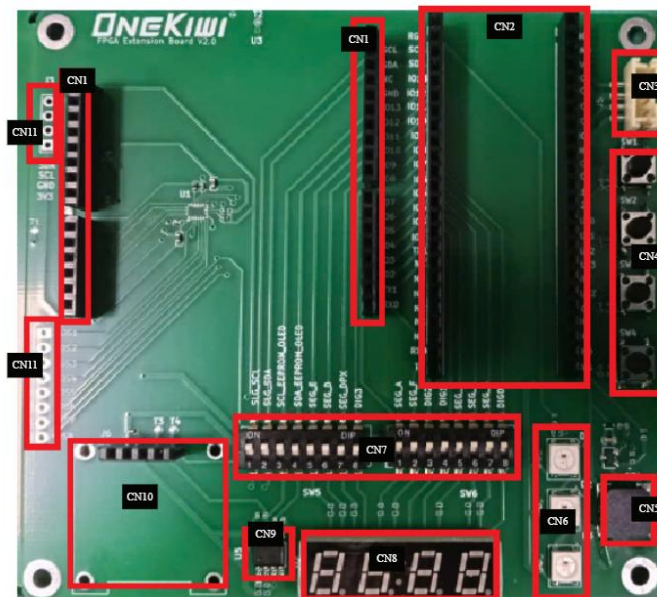


Figure 2-4 Onekiwi 1P5 EVK Components

CN	Name
CN1	Arduino GPIOs Pin header
CN2	Pin header For KIWI 1P5
CN3	Grove
CN4	button
CN5	buzzer
CN6	RGB WS2812
CN7	DIP SWITCH 8
CN8	LED 7 SEGMNETS
CN9	EEPROM IIC
CN10	OLED IIC
CN11	GPIOs

Table 2 EVK components

2.4 System Architecture

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Gowin FPGA 1P5

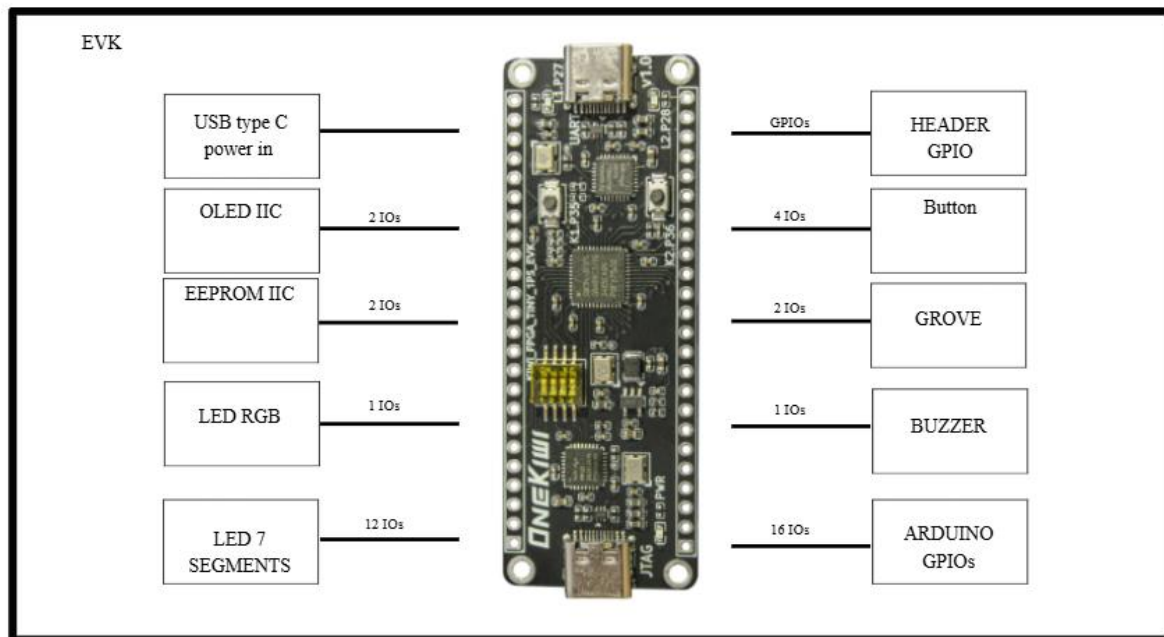


Figure 2-5 System architecture

3.1 FPGA Module

3.2 Connect Kiwi 1P5 and EVK

3.2.1 Pin header for GPIOs Kiwi 1P5

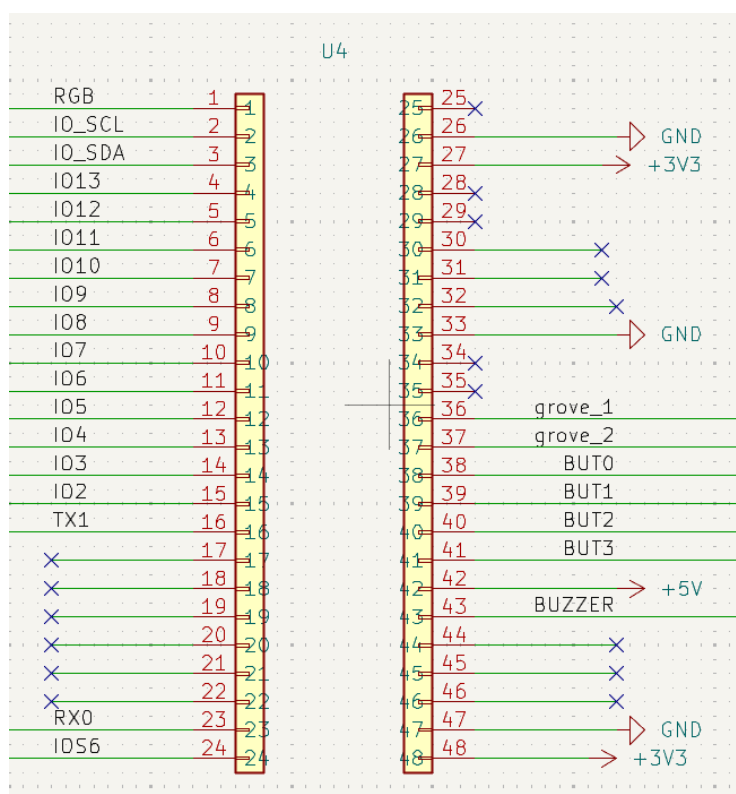


Figure 3-1 Pin header for GPIOs Kiwi 1P5

3.2.2 How to connect

Note: When connect the board 1P5 to EVK , you must connect in right direction before connect Power to 1P5. The USB-Type C for JTAG must be above and USB-Type C for Uart must be below

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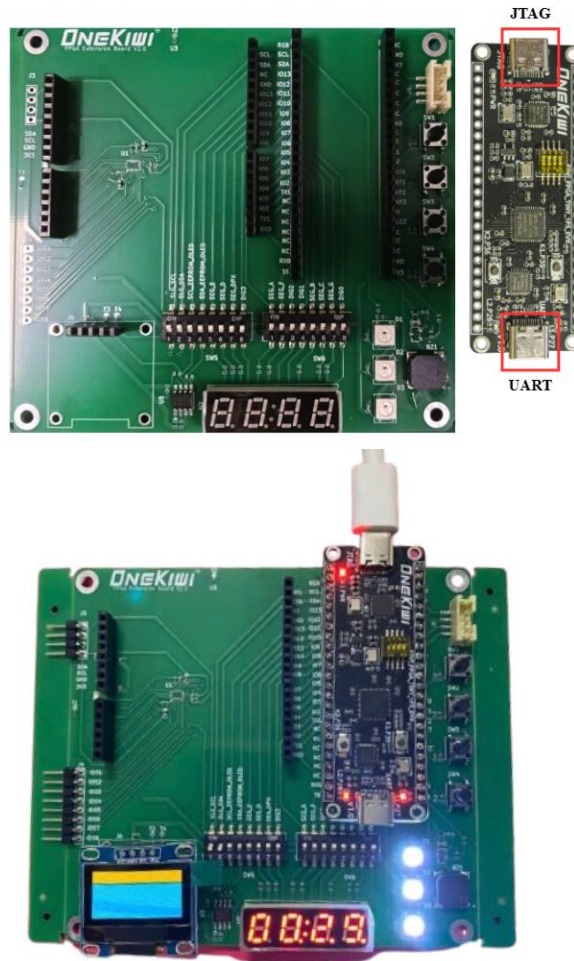


Figure 3-2 EVK right connect with KIWI 1P5 board

3.3 Power Supply(Kiwi 1P5 board)

3.3.1 Overview

The 5V input power interface has overcurrent and inverse current protection. The overcurrent limit is 2A.

The TLV6 power supply chip is used to step down voltage from 5V to 3.3V, The power supply can support up to 2A, which can meet the power demand of the development board.

EVK For Kiwi FPGA 1P5

Gowin FPGA 1P5

3.3.2 Power System Distribution

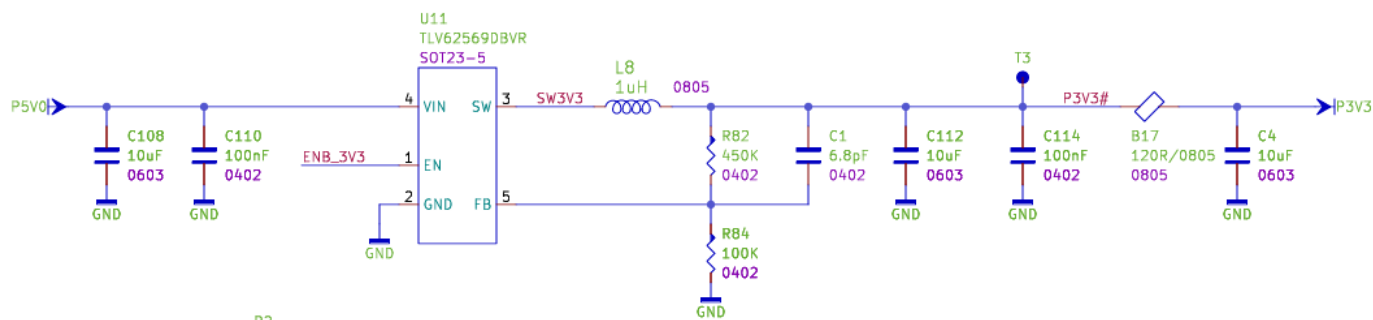


Figure 3-3 Power distribution

3.4 Clock(Kiwi 1P5 board)

3.4.1 Overview

A 27MHz crystal oscillator is provided in the development board that connects to the PLL input pin. This can be employed as the input clock for the PLL in FPGA, and the output clock as needed via multiplication and division of the PLL frequency.

To facilitate testing, a SMA socket is reserved on the development board as the clock input interface. The clock signal is connected to the FPGA global clock pin.

3.4.2 Clock

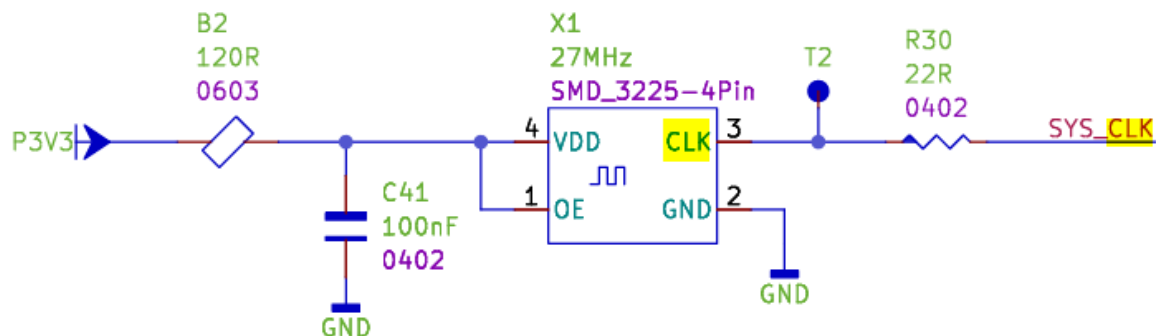


Figure 3-4 Clock circuit

3.4.3 Pinout

Signal Name	Pin No.	BANK	Description	I/O
SYS_CLK	4	0	27 MHz crystal oscillator input	3.3V

Table 3 Pinout Clock

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3.5 LED (kiwi 1P5 board)

3.5.1 Overview

Two green LEDs are incorporated into the development board and are used to display the required status. In addition, Seven LEDs are reserved to signify power supply and FPGA loading status.

Users can test the LEDs in the following ways:

- If the output signal of related pins is logic low, LED is on.
- If logic is high, LED is off.

3.5.2 LED Circuit

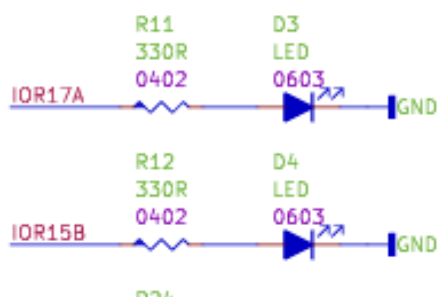


Figure 3-5 Led circuit

3.5.3 Pinout

Signal Name	Pin No.	BANK	Description	I/O
LED1	27	2	LED1	3.3V
LED2	28	2	LED2	3.3V

Table 4 Led pinout

3.6 Key(kiwi 1P5 board)

3.6.1 Overview

Two key switches are embedded in the development board. Users can manually input a low level to the corresponding FPGA pins for testing purposes.

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3.6.2 Key Circuit

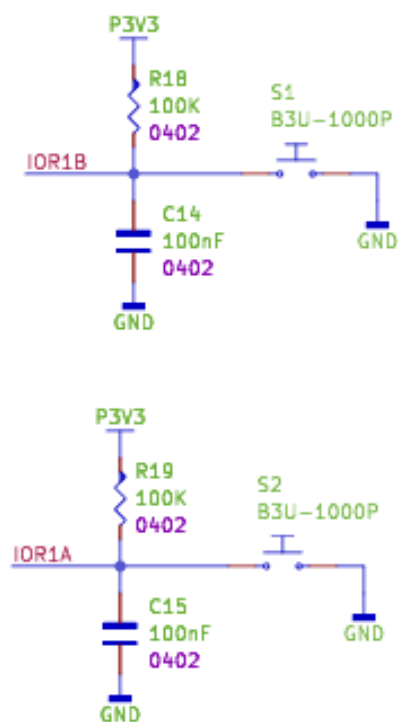


Figure 3-6 Key circuit

3.6.3 Pinout

Signal Name	Pin No.	BANK	Description	I/O
BTN1	35	2	KEY1	3.3V
BTN2	36	2	KEY2	3.3V

Table 5 Key pinout

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3.7 Key(EVK)

3.7.1 Key circuit

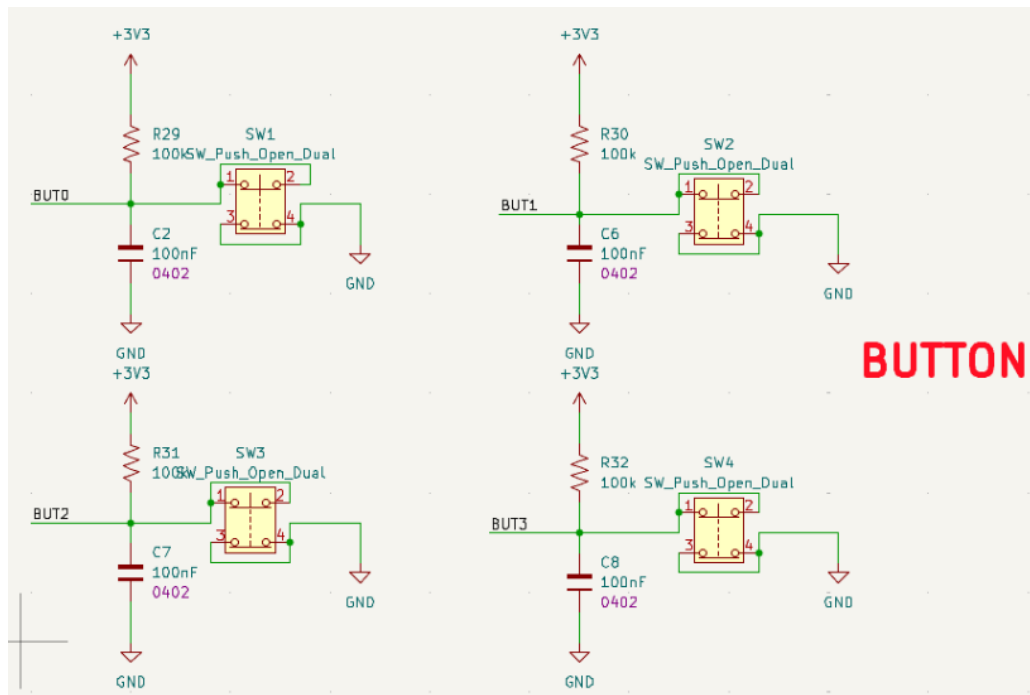


Figure 3-7 Key circuit

3.7.2 Pinout

Signal Name	Pin No.	I/O
BUT0	35	3V3
BUT1	34	3V3
BUT2	33	3V3
BUT3	32	3V3

Table 6 Key pinout

3.8 LED 7 segments

Note: To use LED 7 segments , you must change DIP switch to On.

3.8.1 LED 7 Segments Circuit

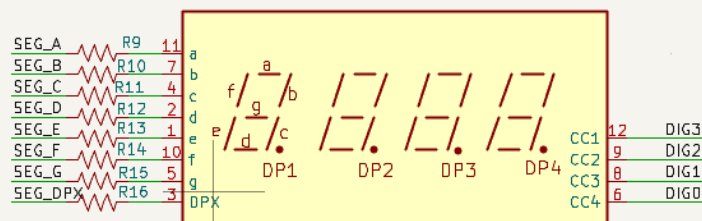


Figure 3-8 LED 7 Segments circuit

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3.8.2 Pinout

Signal Name	Pin No.	I/O
SEG_A	21	3V3
SEG_B	19	3V3
SEG_C	18	3V3
SEG_D	10	3V3
SEG_E	9	3V3
SEG_F	27	3V3
SEG_G	15	3V3
SEG_DPX	11	3V3
DIG0	14	3V3
DIG1	20	3V3
DIG2	28	3V3
DIG3	12	3V3

Table 7 LED 7 Segments Pinout

3.9 EEPROM IIC

3.9.1 EEPROM circuit

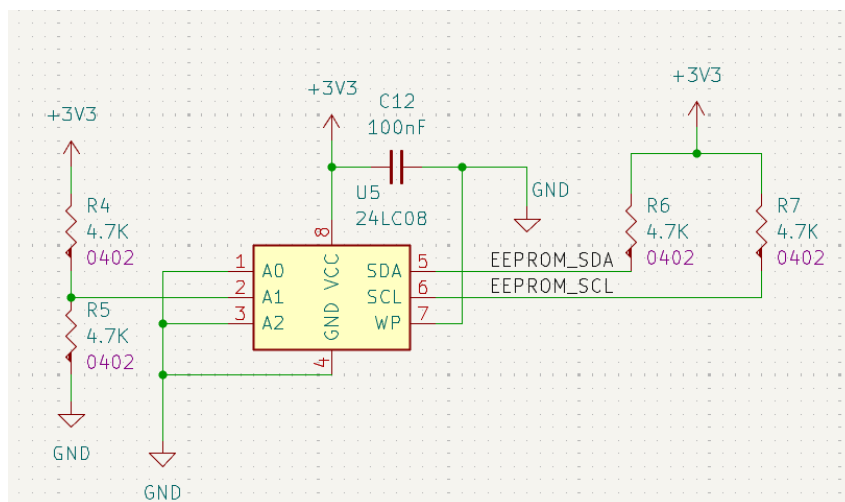


Figure 3-9 EEPROM circuit

3.9.2 Pinout

Signal Name	Pin No.	I/O
EEPROM_SCL	7	3V3
EEPROM_SDA	8	3V3

Table 8 EEPROM circuit

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3.10 RGB Led

3.10.1 RGB Circuit

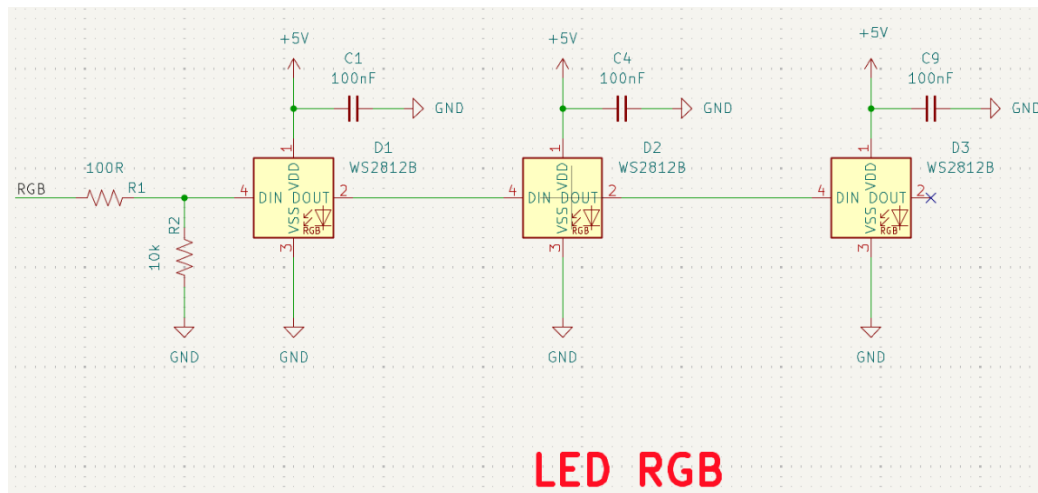


Figure 3-10 RGB Circuit

3.10.2 Pinout

Signal Name	Pin No.	I/O
RGB	2	3.3V

Table 9 RGB pinout

3.11 BUZZER

3.11.1 Buzzer Circuit

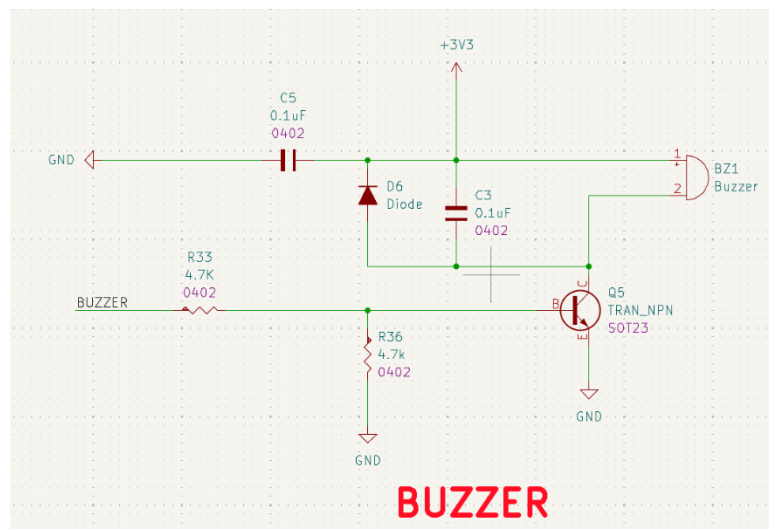


Figure 3-11 Buzzer Circuit

3.11.2 Pinout

Signal Name	Pin No.	I/O
Buzzer	36	3.3V

Table 10 Buzzer pinout

3.12 OLED IIC

The I2C Wires of OLED are the same with EEPROM.

3.12.1 OLED circuit

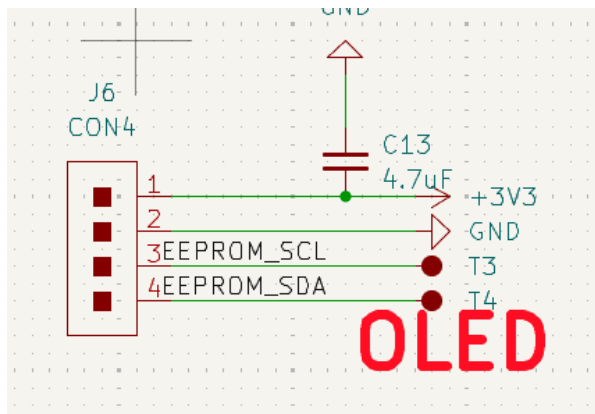


Figure 3-12 OLED circuit

3.12.2 Pinout

Signal Name	Pin No.	I/O
EEPROM_SCL	7	3V3
EEPROM_SDA	8	3V3

Table 11 Oled pinout

3.13 Grove

3.13.1 Grove circuit

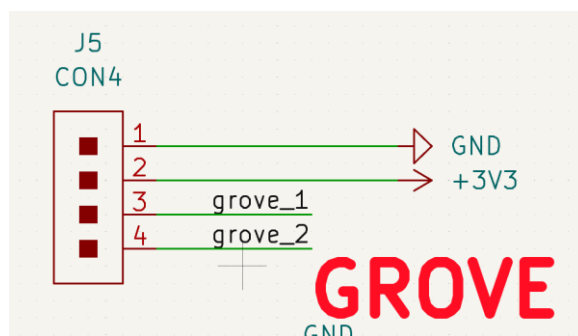


Figure 3-13 Grove circuit

3.13.2 Pinout

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Signal Name	Pin No.	I/O
grove_1	29	3V3
grove_2	31	3V3

Table 12 Grove table

3.14 Arduino Pin header

3.14.1 Arduino Pin header circuit

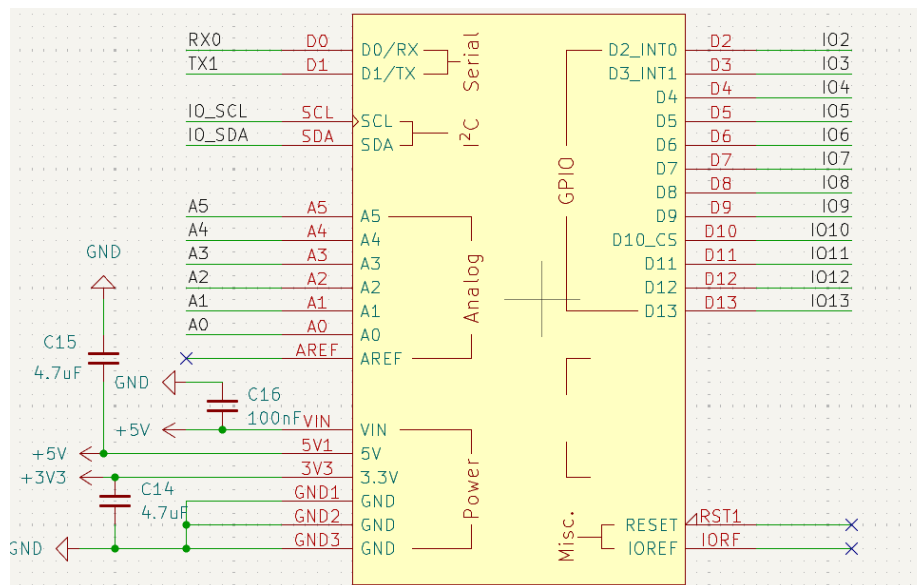


Figure 3-14 Grove circuit

3.14.2 Pinout

Signal Name	Pin No.	I/O
IO_SCL	3	3V3
IO_SDA	5	3V3
IO13	7	3V3
IO12	8	3V3
IO11	9	3V3
IO10	10	3V3
IO9	11	3V3
IO8	12	3V3
IO7	14	3V3
IO6	15	3V3
IO5	18	3V3
IO4	19	3V3
IO3	20	3V3
IO2	21	3V3
TX1	26	3V3
RX0	27	3V3

Figure 3-15 Grove pinout

3.15 Pin headers

The CON 8 header used for debug analog signal SLG4686, so may be you do not use it.

The CON 4 header you can use when change DIP SWITCH signal SLG_SCL AND SLG_SDA to ON.(It use the same IO with arduino header IO_SCL and IO_SDA)

3.15.1 Gpio circuits

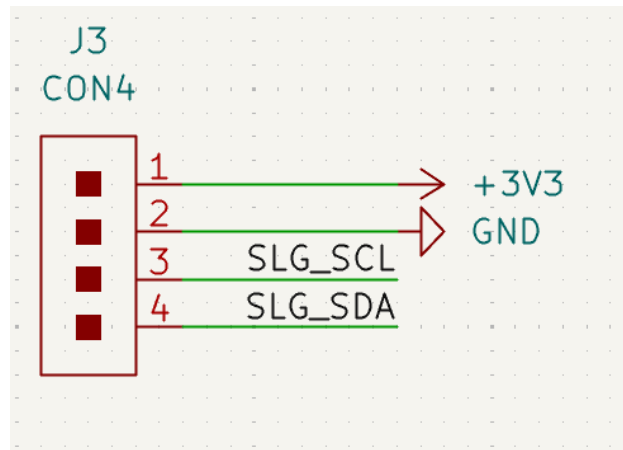


Figure 3-16 Gpio circuit

3.15.2 Pinout

Signal Name	Pin No.	I/O
SLG_SCL	3	3V3
SLG_SDA	5	3V3

Figure 3-17 GPIO pinout

4 Consideration

Considerations for the use of the development board:

1. Handle with care and pay attention to electrostatic protection.
2. When downloading bitstream files to internal flash or external flash, set the MODE pin state to the correct configuration value, please refer to: <https://cdn.gowinsemi.com.cn/UG290E.pdf>
3. Power input 5V